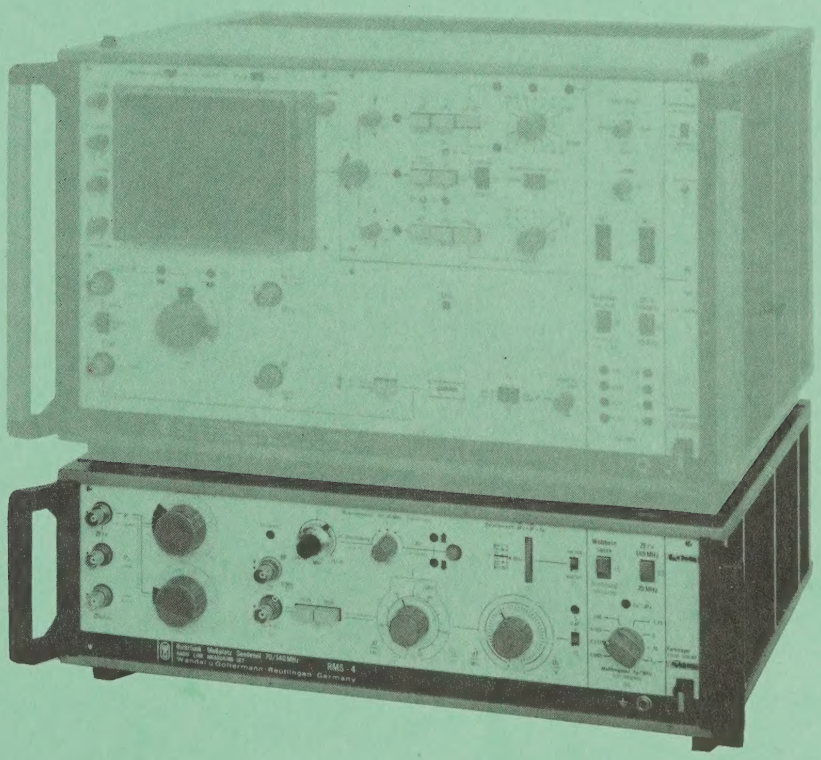
Service Manual



MP MASTER
MA29309

Send Section

RMS-4

of the Radio-Link Measuring Setup RM-4

SEND SECTION RMS-4

of the Radio-Link Measuring Set-up RM-4

Service Manual 696 G...

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- Important safety precautions

This measuring instrument was dispatched from the factory in perfect condition, and that statement includes the built-in safety features. To maintain these features, as intended, for perfectly safe operation of the instrument, we suggest that the following advice be very carefully taken into account.

- Opening the instrument enclosure

When the enclosure is opened, or if components are removed, certain voltage carrying components could be exposed, also connection points might be carrying voltages.

Therefore, all voltage sources must be disconnected before the enclosure is opened.

If opening an instrument cannot be avoided, however, when it must have operating voltage applied as for calibration, maintenance or repair, then only an experienced person should undertake the task because knowledge of the dangers involved is required as a precaution.

Charged capacitors are dangerous even after the instrument has been disconnected from voltage sources; the circuit diagrams should be used for locating such dangerous points.

- Fuses

Only the prescribed fuses may be used (no substitute values)

- Repairs, substitution of components

Repairs should be made according to accepted technical standards. Moreover, particular pains must be taken to maintain the protective features as originally designed in the instrument. That means, changes must not be made if there is any chance of decreasing protection. Especially important are leakage paths and air gaps and separations due to insulation, these must not be decreased.

Only use original components for replacement. Other repair components are permissible only if the safety/protective features of the instrument are not degraded.

- Tests after repair and maintenance

Testing the protective ground connection

The correct connection and first-rate function is checked by visual inspection and through measurement of the resistance between the instruments enclosure and the protective ground connection at the power plug.

The resistance should be less than 0.5 Ω. During this resistance measurement, the power cord should be repeatedly moved (wiggled). Changes in resistance indicate a damaged connection or power cord.

- Checking the insulation resistance

The insulation resistance should be measured with 500 V d. c. applied between the a. c. power cord connectors and the protective ground conductor. For this, the a. c. power switch of the instrument should be switched to ON. The Insulation resistance should be greater than 2 MΩ.

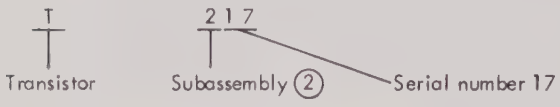
6. PRELIMINARY REMARKS TO SERVICE MANUAL

The following sections 6.1. to 6.5. explain the applied abbreviations, symbols and schematics as used in the "Service Handbook" (Service Manual and Appendix including circuit diagram, layout drawings and component lists).

The tabulated list of applied measurement items in section 6.6. presents the minimum complement of measurement equipment needed for all the measurements suggested in the Service Manual.

6.1. COMPONENT DESIGNATION

The various subassemblies are annotated with an individual number, for instance (2) Input amplifier. Each component located in this subassembly has the number 2 as its first digit. The two subsequent digits define the serial number of the component; for instance, resistor 96 would be R 296, or diode 22 is GI 222 and so on. The prefix letter characterises the type of component.

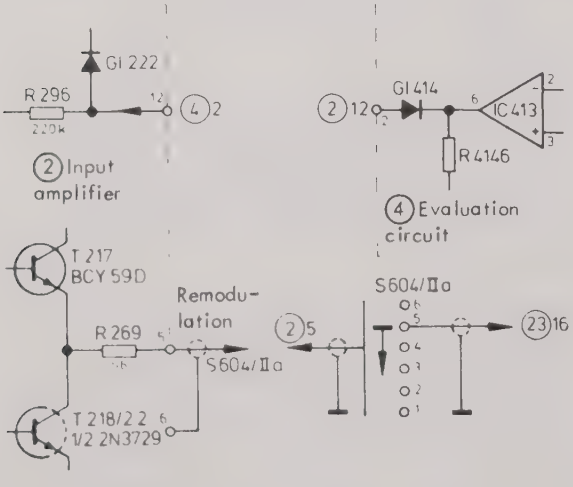


The abbreviations used to designate the components are given in section 6.3.

6.2. INTERCONNECTION BETWEEN SUBASSEMBLIES

Since the circuit diagrams are given separately for each subassembly, it is important that all interconnections are shown clearly. The following drawing explains the method used in this manual.

In the sketch below, point 12 of module (2) is connected to point 2 of module (4), and there is a shielded connection from point 5 of module (2) to switch S 604/IIa of subassembly (6).



6.3. ABBREVIATIONS AND SYMBOLS

In order to achieve greater simplicity, the following abbreviations and symbols have been used in the text and on the circuit diagrams:

6.3.1. Discrete components

Battery	B	
Socket	Bu	
Diode, rectifier	GI	
Zener diode	G	
LED	GI	
Thyristor	GI	
Varactor diode	GI	
Inductance	L	
Meter	J	
Capacitor	C	
Potentiometer	P	
Quartz crystal	Q	
Relay	Rel	
Relay contact	rel	
Resistor	R	
Thermistor PTC resistor	R	
Switch	S	
Fuse	Si	
Control lamp	SL	
Transistor	T	B E
Transistor (FET)	T	D S G
Transformer	Ü	

Other important abbreviations:

(2) = subassembly (2) = circuit diagram (2)

607-L = Printed circuit board "L"

point 6 = Circuit reference/connection No. 6

TP 302 = Test point 302 (in subassembly (3))

6. PRELIMINARY REMARKS TO SERVICE MANUAL

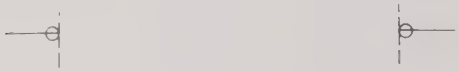
6.3.2. Digital symbols

In the following, some of the most important digital logic-switching symbols are given, although the list is not presented as complete.

The two possible states of binary logic are designated "L" (low) and "H" (high). The voltages corresponding to each state are defined as being closer to $-\infty$ for the "L" range and closer to $+\infty$ for the "H" range.

6.3.2.1. General symbols

Symbol for negation of an input or output:



The dashed line represents the boundary line of the circuit.

Symbol for dynamic input

a) The operation is such that a transition of the input signal from L to H produces an effect similar to a "H" pulse

b) As in a) except operation effective on a H to L transition

Trigger inputs (G inputs)

Static control

operates with a "H" signal — G

operates with a "L" signal — G

one transition control

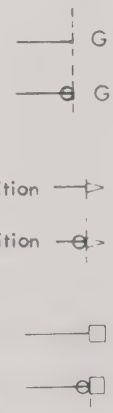
operates with a L - H transition — G

operates with a H - L transition — G

two transition controls

operates with a L-H-L pulse

operates with a H-L-H pulse



Preparatory inputs

EX — EX = preparing input

X — X = triggering input

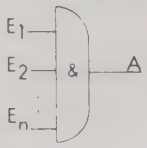
The circuit delivers a "H" pulse when the signal at X transits from L to H, providing a "H" signal is already present at input EX.

Same as above. However, operative when signal at X input transits from H to L.

Note: Any storage time is to be noted (EX) !

6.3.2.2. Digital signal gates

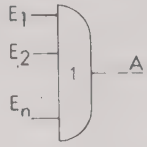
The AND gate



An "H" signal appears at output A only when an "H" signal is applied to all the inputs simultaneously. (Conjunction AND gate)

E_1	E_2	A
L	L	L
L	H	L
H	L	L
H	H	H

The OR gate



An "H" signal appears at the output when at least one input has an "H" applied to it. (Disjunction)

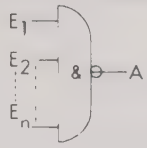
E_1	E_2	A
L	L	L
L	H	H
H	L	H
H	H	H

The NOT gate

The input signal always appears inverted at the output (Inverter)

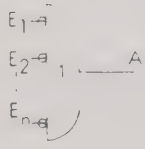
E	A
H	L
L	H

The NAND gate



An L signal appears at the output when an "H" signal is fed in at all inputs

E_1	E_2	A
L	L	H
L	H	H
H	L	H
H	H	L

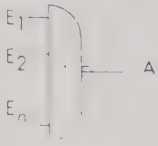


Alternative symbol
De Morgan's rule states the alternative symbol is true whereby:

$$A = \overline{E_1 \wedge E_2 \wedge \ldots E_n}$$

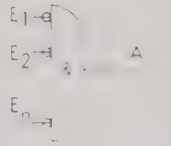
$$A = \bar{E}_1 \vee \bar{E}_2 \vee \ldots \bar{E}_n$$

The NOR gate



An L signal appears at the output, when at least one input has an "H" applied

E_1	E_2	A
L	L	H
L	H	L
H	L	L
H	H	L



Alternative form
According to De Morgan's rule:

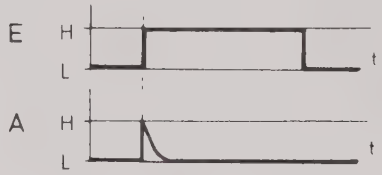
$$A = \overline{E_1 \vee E_2 \vee \ldots E_n}$$

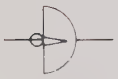
$$A = \bar{E}_1 \wedge \bar{E}_2 \wedge \ldots \bar{E}_n$$

6. PRELIMINARY REMARKS TO SERVICE MANUAL

Differentiators

Symbol for circuits which convert a L-H transition into a L-H-L needle pulse





Symbol for circuits which convert a H-L transition into a H-L-H needle pulse

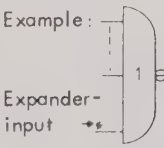
Wired AND

The symbol "wired AND" signifies that two or more circuits are wired in such a way that it simulates an AND logic without actually using an AND logic element

NOR Gate with power fan out

Where the logic element is capable of being loaded, the boundary line at the output side is drawn thick. This signifies that the output from this module is capable of driving several other modules simultaneously. In IC technology this is described as "fan out" capability.

Extending the input circuit by means of an "Expander" input



NOR circuit with four inputs. A further special input permits extending the logic circuit through external circuitry.

6.3.2.3. Bistable circuits with memory behavior

Two different basic types are discussed here: the Flip-Flop (FF) and the monostable (MF)

Flip-Flops

These toggle circuits have two stable states: Depending on the input signal, the flip-flop assumes one of the two states.

If one of the two states is defined as the normal position, then that output which assumes the H status is identified by a block bar.

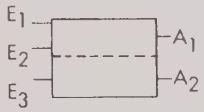
Static input signals (explanation and example)

If the signal at input E_1 changes from L to H, then the FF toggles, independently of the slope of the L-H transition, to the status which is identified by an H status at output A_1. Thus, output A_2 is forced to be in the L status.

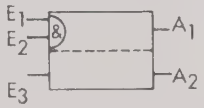
If the signal at input E_1 changes from H to L, then the FF remains in the previously assumed state. Only after the signal changes from L to H at input E_2, does the FF toggle to the second stable status identified by an H status at output A_2, (here taken as the normal position). Output A_1 is then forced to assume L status.
This state is maintained by the FF even though the signal at input E_2 may change from H to L.
Generally it is impermissible, to apply L-H transition signals simultaneously to inputs E_1 and E_2.

E_1	E_2	A_1	A_2	
H↓	L	H	L	
L↓	L	H↑	L	
L	H↓	L↓	H↑	
L	L	L	H	
H↑	L	H↑	L↓	
H	H↓			no FF action

If a flip-flop has several inputs without special identifications, then these inputs are disjunctive-coupled (OR gate).
That means:
The flip-flop toggles with a transition from L to H at inputs E_1 or E_2, or at both; the state becomes that identified by an H status at output A_1.

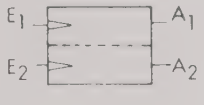


In the following symbol, the inputs E_1 and E_2 are conjunctive-coupled (AND gate).
That means:
The flip-flop first toggles when the two inputs E_1 and E_2 simultaneously assume the H status



Examples with dynamic signals at the inputs

The symbol represents a FF with two dynamic inputs E_1 and E_2. A L-H transition at input E_1 toggles the Flip-Flop to the state identified by an H appearing at A_1. Similarly a L-H transition at E_2 toggles the Flip-Flop to the state identified by an H appearing at A_2.

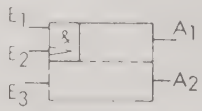


6. PRELIMINARY REMARKS TO SERVICE MANUAL

A symbol ⊳ (or ⊲) shown against the dashed line signifies that the Flip-Flop toggles from one stable state to the other alternately at each L-H (orH-L) transition. Thus an H (or L) appears alternately at A_1 and A_2.

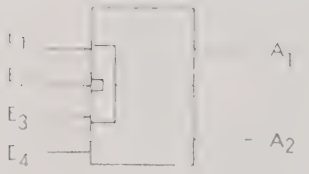
Flip-Flops with preparatory inputs

This Flip-Flop reacts to a L-H transition at the dynamic input E_2 only if simultaneously an H signal is present at input E_1. In this case the Flip-Flop toggles to the state in which an H appears at output A_1. E_3 is a static input.



In the following switching symbol, the dynamic input reacts when the two other inputs have been prepared, i.e. every L-H transition at input E_2 toggles the flip-flop when at the same time an H status exists at input E_1.

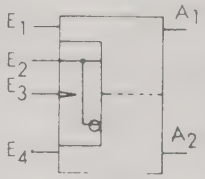
J-K Master Slave Flip-Flop (e.g. SN 7473 from Texas Instruments)



t_n		$t_n + 1$	
E_1	E_3	A_1	A_2
L	L	A_{1_n}	A_{1_n}
L	H	L	H
H	L	H	L
H	H	$\bar{A}_{1_n}$	A_{1_n}

t_n : point of time prior to clock pulse
$t_n + 1$: point of time after clock pulse
E_2 : clock input
E_4 : non-synchronous reset input (independent from E_2)
"L" at E_4 forces A_1 to "L"

D Type Flip-Flop (edge-triggered) (also as on example of the SN 7474 from Texas Instruments)



Flip-Flop with preparing input E_2 and a higher ordered triggering input E_3

E_1 and E_4 are directly effective at the outputs.

t_n	$t_n + 1$	
E_2	A_1	A_2
L	L	H
H	H	L

Monostable circuits

These also known as one-shot multivibrators. They have only one stable state (normally open) and a quasi-stable state (closed); whereby the arrow is drawn to show which output is in the normally closed state.

Example:
In the following monostable, an L status applied to the static input E_1, or a L-H transition at the dynamic input E_2, toggles the circuit from the normally open status to become the quasi-stable closed status (Hstate at output A_1)

After the retoggle time t_R, whose period is determined by an internal RC network, the monostable toggles back to the normally open status.

6.3.2.4. Delay networks

Delays the transition from L to H

Delays the transition from H to L

The transition from L to H as well as the transition from H to L are delayed, but the delay times are different

The transition L to H and from H to L are delayed by the same amount

The double slant stroke identifies the input side.

The delay time can be noted on the symbol in units of time, e.g. ms or µs.

7. INSTRUCTIONS FOR FAULT FINDING AND REPAIR

The following sections contain all information necessary for fault finding and localization. The main emphasis in fault finding should be location of functional faults and not of tolerance errors, whereby tolerance errors are defined as values outside a guaranteed error limit without serious effects on the equipment function.

Fault finding is carried out with the aid of fault finding and level diagrams and with oscillograms of various signals. Two tables describe the function of the switches on the front and rear sides of the equipment, and their effects on the various assemblies and components. These tables are a useful aid for fault finding as they make it clear that most switches act on several assemblies or components. This is not easily seen from the circuit diagrams.

A further aid for fault finding is the Appendix to the operating and servicing instructions, containing block diagrams, circuit diagrams, component location drives, and parts lists. Chapter 10, FUNCTIONAL DESCRIPTION, explains the circuit diagrams.

In addition, all photographs of all important aspects of the units and pictures show in the position of assemblies and test points are provided in the following sections to simplify fault finding.

For repair work, disassembly instructions in Section 7.4. should be observed.

7.1. Preparing the unit for fault finding

For fault finding, the cover, the baseplate, and the left sidewall should be removed. It is best to place the unit on its right sidewall (with power supply) for this purpose.

The enclosed hexagon wrench (SW3), which is held in a clip on the rear of the unit, should be used for loosening the hexagon head cap screws which fix the cover and the baseplate to the sidewall.

After removal of the various parts of the case, the equipment chassis with the circuit boards is accessible. If necessary, the screening covers on the printed circuit boards can be lifted off with the loops provided for this purpose.

The frequency regulation assembly (board 696-S...) which is located between the upper and lower mounting boards, can be pulled out, after lifting up a retaining clip, sufficiently to provide access to the components on the board after removal of the cover. The board is locked into the withdrawn position.

Note: Before opening the unit and in particular before pulling out the board 696-S..., ensure that the unit is switched off and the mains plug removed from the outlet socket.

7.2. Position of test points, adjustment components, and assemblies in the unit

Figure 7-1 and 7-2 show the positions of the test points required for fault finding. The various assemblies whose identification is made difficult be removal of the screening covers with the printed board designation are also marked. All components used for adjustment purposes are identified.
A unit of the B series was used for the photographs.

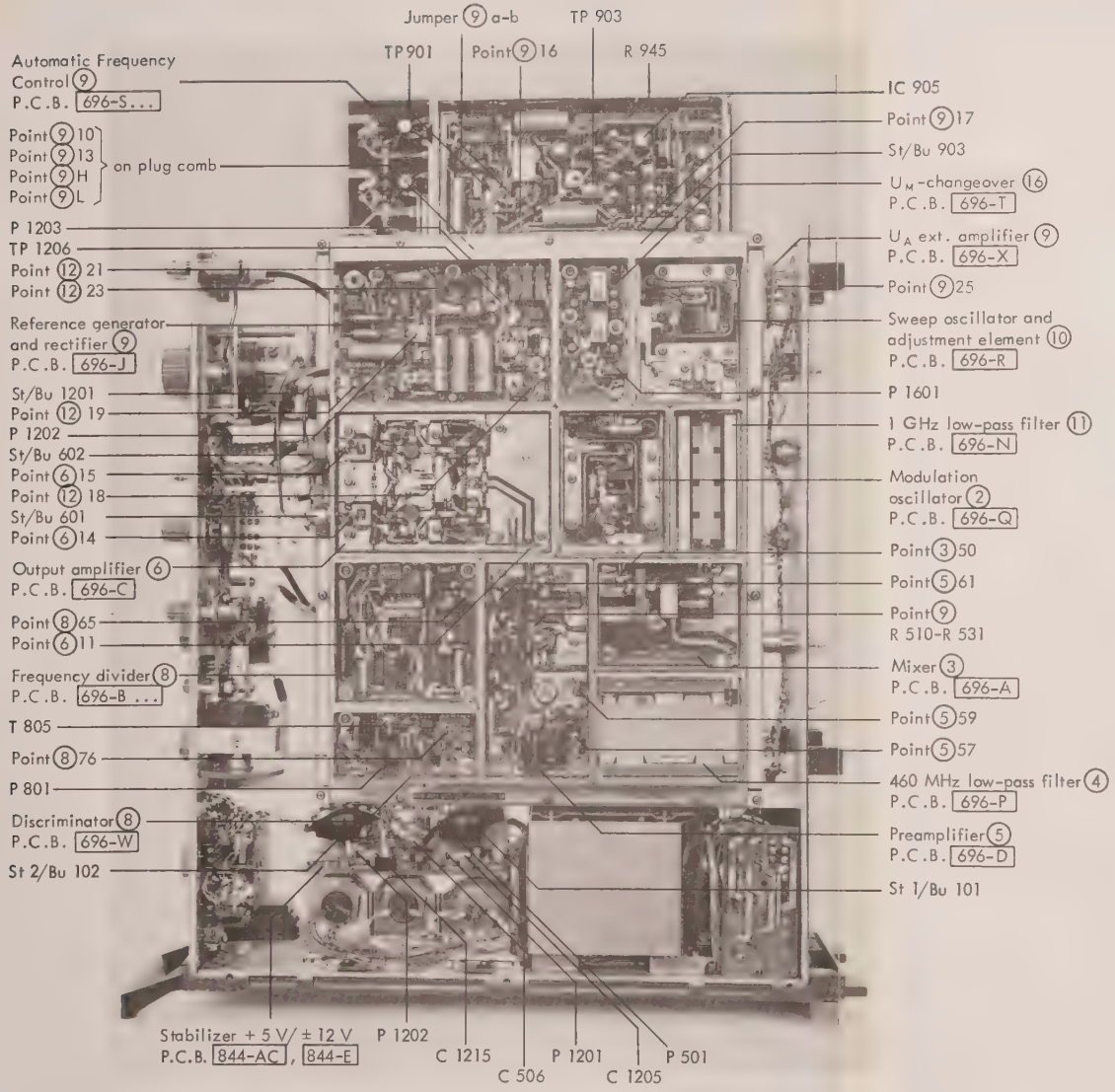


Fig. 7-1 Send section RMS-4: viewed from above, instrument placed on its right side

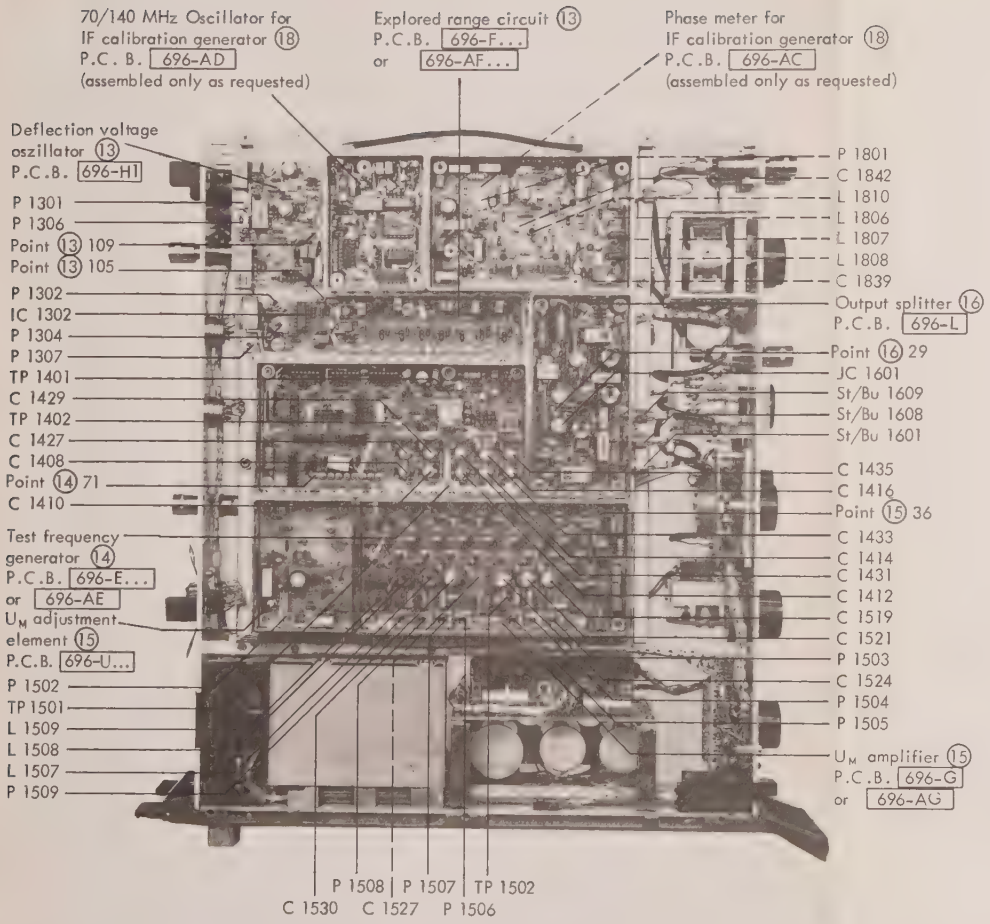


Fig. 7-2 Send section RMS-4: viewed from below, instrument placed on its right side

7.3. Fault finding

7.3.1. Checking the supply voltages

The DC supply voltages can be checked on the regulator boards 844-E and 844-AC of the power supply unit. Measurements are carried out at the test points specified in the Table 7-1.

Required test equipment:
1 Digital voltmeter e.g. 8000 A, Fluke

Supply voltage	Measured across
+12 V ± 0.5 %	C 1205
+12 V ± 0.5 %	C 1215
+ 5 V ± 0.5 %	C 506

Table 7-1 Test points for checking the DC supply voltages

7.3.2. Fault finding in the IF section

Defects in the IF section of the RMS-4 lead to two types of faults:
Either the IF level or the intermediate frequency (IF center frequency, sweep range, IF shift) is incorrect.

However, it is also possible that a fault in the level control circuit causes the frequency control circuit to operate incorrectly and vice versa. The reason for this is the overlap of the two control circuits. However, fault finding should always be started with the frequency control circuit as the IF frequency must be correct for checking of the level control circuit.

Before starting fault finding, check that the controls of the unit are correctly set. In particular, check the following questions:

- Correct IF center frequency selected with switch [9] (S 903)?
- Swtich [4] (S 803) in position "Center frequency" 70/140 MHz?
- Correct operating mode (sweep or wideband) selected?
- U_A, U_M int. operation selected with switch [34] (S 901) on the rear of the unit?
- Explored range switch [7] (S 1301) switched off?

7.3.2.1. Fault finding diagrams

Fault finding is carried out with the aid of fault finding diagrams, which are used in the following manner: If the question in a fault finding step is answered with "YES", then follow the line upwards to the next step. If the question is answered with "NO", follow the line downwards. In the case of fault finding steps marked with a number, the corresponding note should be observed.

If fault finding with the fault finding diagram is not successful, a further aid is provided in the form of level diagrams, in which the required levels and voltages which exist at various test points when the equipment is operating correctly are specified.

Test equipment required for fault finding:
1 DC power supply (up to 20 V) e.g. GS-2 W&G
1 Digital frequency meter (up to 2 MHz) e.g. FZ-4 W&G
1 Digital voltmeter e.g. 8000 A Fluke
1 Millivoltmeter with VHF probe e.g. 411 A with probe 11023 A hp
1 Spectrum analyzer e.g. 8558 B/182 T hp
1 Oscilloscope with 10:1 probe e.g. PM 3240 with probe PM 9350 Philips

Basic settings on the RMS-4 before starting fault finding with the aid of the fault finding diagrams:

[2] (P 1201) [13] (EL 601)	:	0 dBm
[4] (S 803)	:	Center frequency 70/140 MHz
[8] (S 902)	:	Sweep
[9] (S 903)	:	70 MHz
[16] (P 1501)	:	Fully anticlockwise
[17] (P 1305)	:	Fully anticlockwise

Notes on the fault finding diagram "Frequency control circuit"

[1.]

Set up the test configuration shown in Figure 7-3:

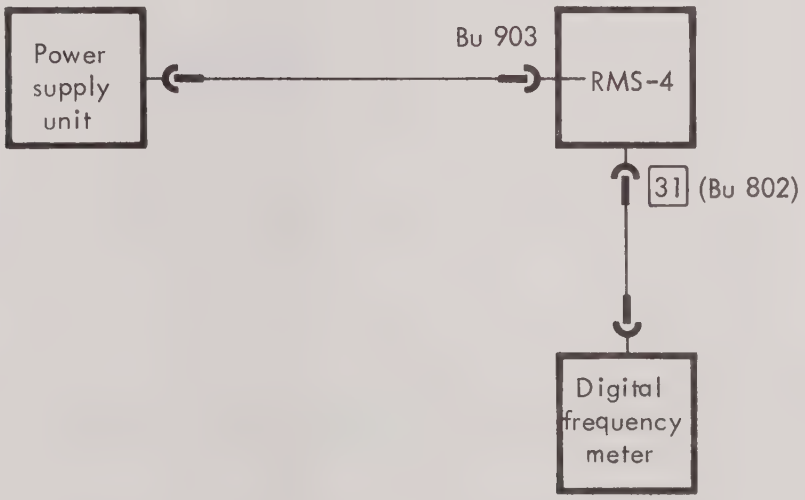


Figure 7-3

The subminax connector St/Bu 903 is accessible if the board [696-S...] (see also Figure 7-2) is completely removed from its guides!
The DC voltage injected at socket Bu 903 is to be varied as shown in Figure 7-4.

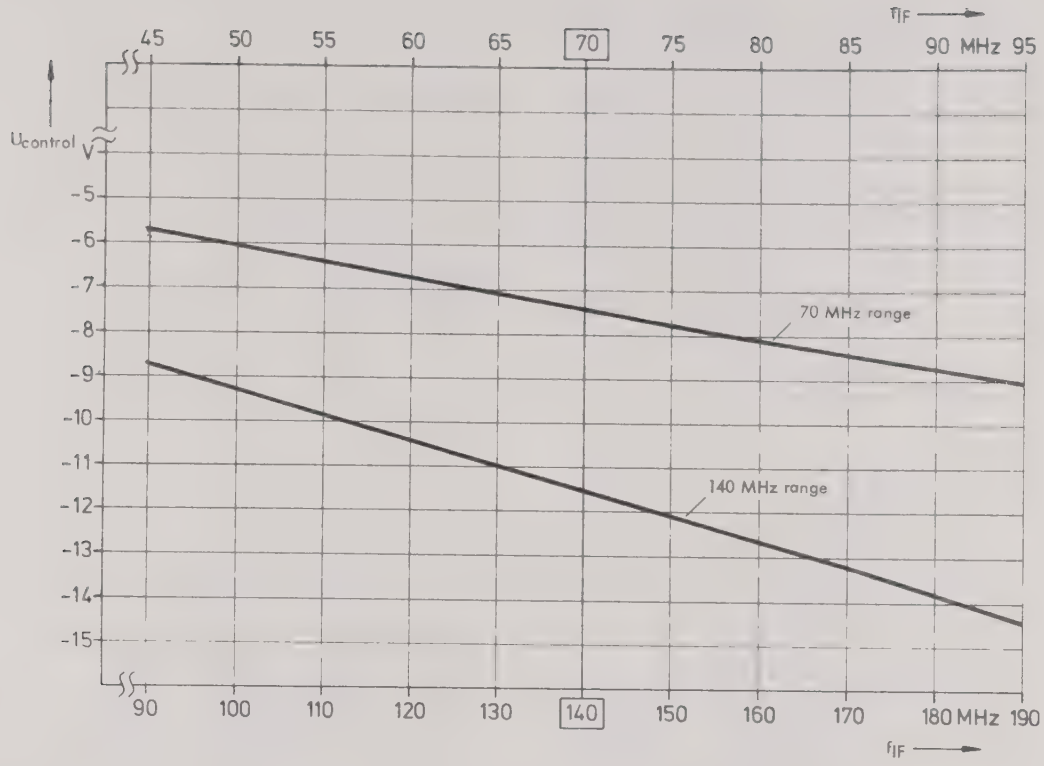
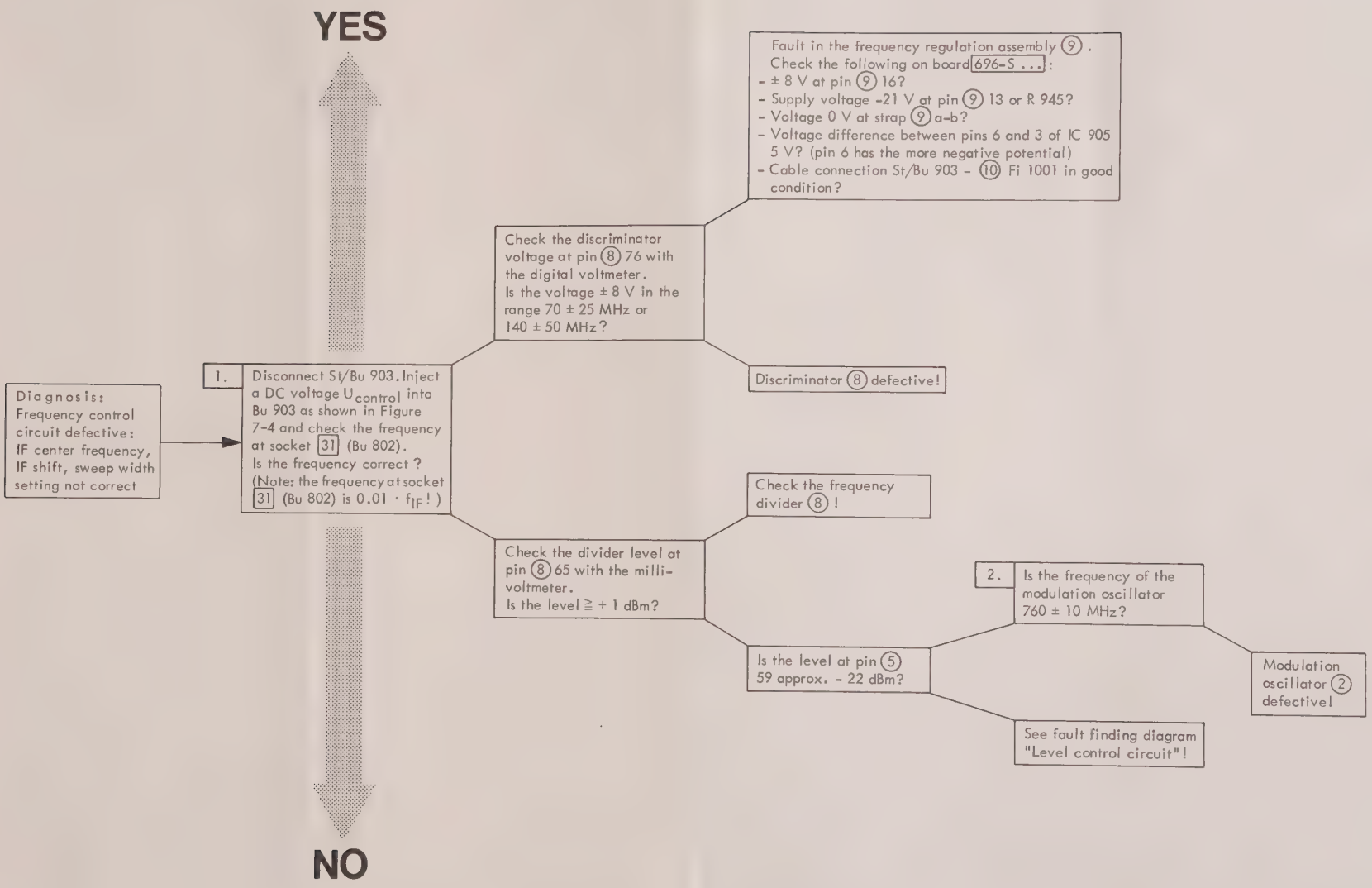


Figure 7-4 Control voltage for the sweep oscillator (10)

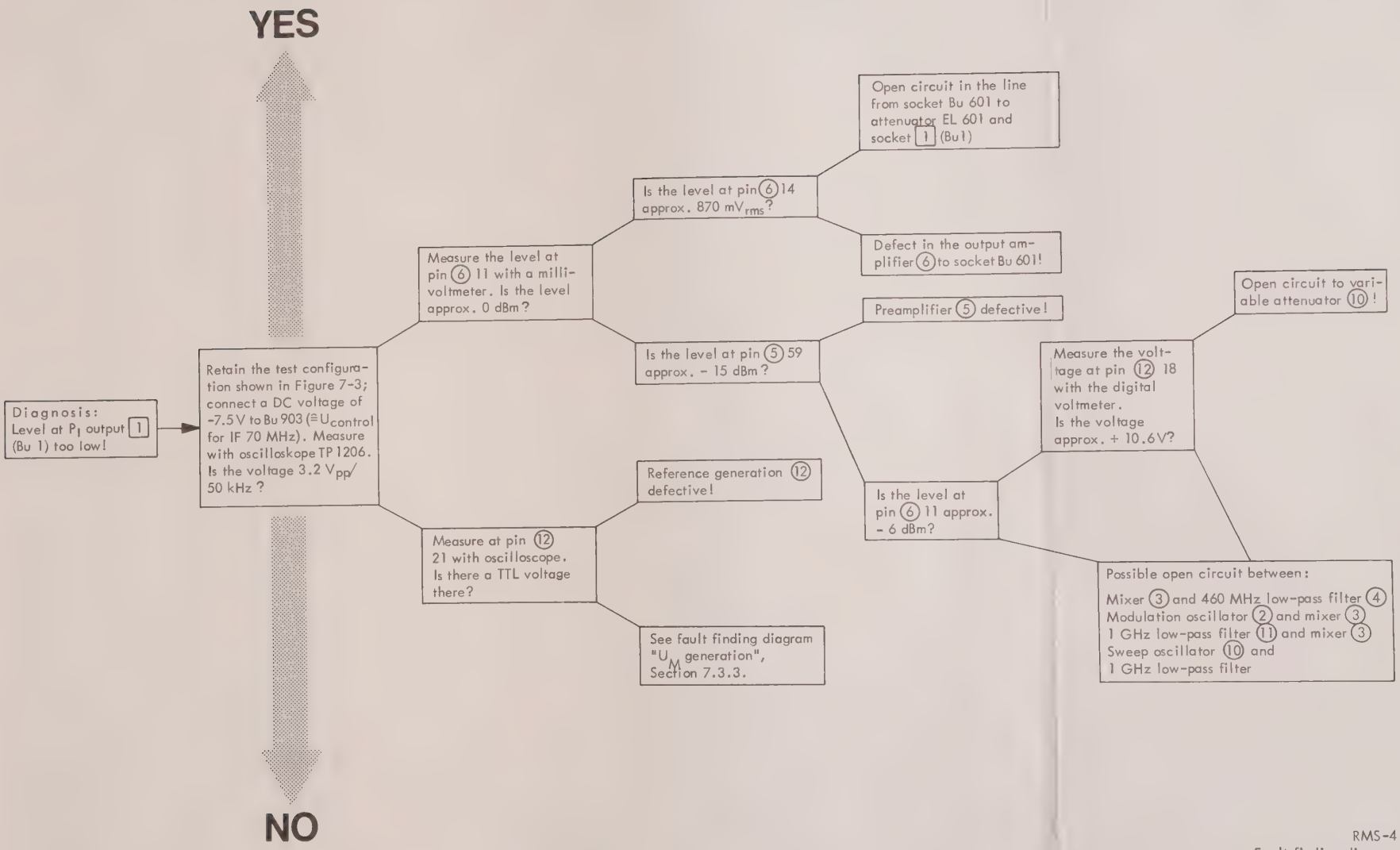
2.

Measurement is carried out with the spectrum analyzer, whose frequency axis should be calibrated beforehand.

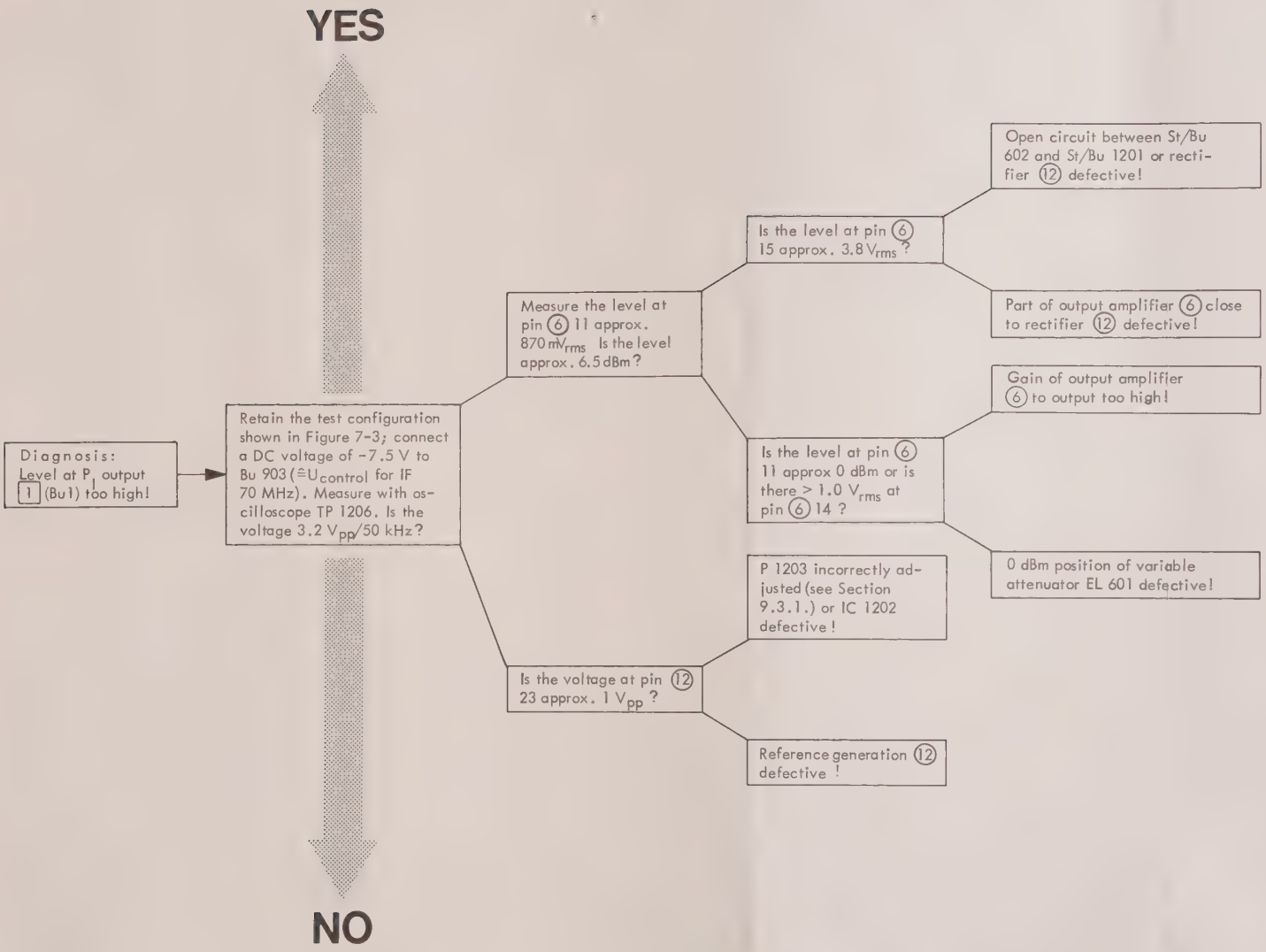
Before carrying out measurements, hold the open end of the cable leading to the analyzer in the vicinity of pin (3) 50 - with the cover of mixer (3) open; the cover of the modulation oscillator (2) remains closed


YES
Diagnosis:
Frequency control circuit defective:
IF center frequency, IF shift, sweep width setting not correct
1.
Disconnect St/Bu 903. Inject a DC voltage $U_{control}$ into Bu 903 as shown in Figure 7-4 and check the frequency at socket 31 (Bu 802).
Is the frequency correct ?
(Note: the frequency at socket 31 (Bu 802) is $0.01 \cdot f_{IF}$!)
Check the discriminator voltage at pin 8 76 with the digital voltmeter.
Is the voltage ± 8 V in the range 70 ± 25 MHz or 140 ± 50 MHz?
Fault in the frequency regulation assembly 9.
Check the following on board 696-S ... :
- ± 8 V at pin 9 16?
- Supply voltage -21 V at pin 9 13 or R 945?
- Voltage 0 V at strap 9 a-b?
- Voltage difference between pins 6 and 3 of IC 905 5 V? (pin 6 has the more negative potential)
- Cable connection St/Bu 903 - 10 Fi 1001 in good condition?
Discriminator 8 defective!
Check the divider level at pin 8 65 with the millivoltmeter.
Is the level ≧ + 1 dBm?
Check the frequency divider 8 !
2.
Is the frequency of the modulation oscillator 760 ± 10 MHz?
Modulation oscillator 2 defective!
Is the level at pin 5 59 approx. - 22 dBm?
See fault finding diagram "Level control circuit"!
NO

RMS-4
Fault finding diagram
Frequency control circuit


YES
Diagnosis:
Level at P_1 output [1] (Bu 1) too low!
Retain the test configuration shown in Figure 7-3; connect a DC voltage of -7.5 V to Bu 903 (≙ $U_{control}$ for IF 70 MHz). Measure with oscilloskope TP 1206. Is the voltage 3.2 V_{pp}/ 50 kHz ?
Measure the level at pin (6) 11 with a millivoltmeter. Is the level approx. 0 dBm?
Is the level at pin (6) 14 approx. 870 mV_{rms}?
Open circuit in the line from socket Bu 601 to attenuator EL 601 and socket [1] (Bu1)
Defect in the output amplifier (6) to socket Bu 601!
Is the level at pin (5) 59 approx. - 15 dBm?
Preamplifier (5) defective!
Is the level at pin (6) 11 approx. - 6 dBm?
Measure the voltage at pin (12) 18 with the digital voltmeter. Is the voltage approx. + 10.6 V?
Open circuit to variable attenuator (10)!
Possible open circuit between:
Mixer (3) and 460 MHz low-pass filter (4)
Modulation oscillator (2) and mixer (3)
1 GHz low-pass filter (11) and mixer (3)
Sweep oscillator (10) and
1 GHz low-pass filter
Measure at pin (12) 21 with oscilloscope. Is there a TTL voltage there?
Reference generation (12) defective!
See fault finding diagram "U_M generation", Section 7.3.3.
NO

RMS-4
Fault finding diagram
Level control circuit
Part 1


YES
Diagnosis:
Level at P_1 output
1 (Bu1) too high!
Retain the test configuration shown in Figure 7-3; connect a DC voltage of -7.5 V to Bu 903 (≙$U_{control}$ for IF 70 MHz). Measure with oscilloscope TP 1206. Is the voltage 3.2 V_{pp}/50 kHz?
Measure the level at pin (6) 11 approx. 870 mV_{rms} Is the level approx. 6.5 dBm?
Is the level at pin (6) 15 approx. 3.8 V_{rms} ?
Open circuit between St/Bu 602 and St/Bu 1201 or rectifier (12) defective!
Part of output amplifier (6) close to rectifier (12) defective!
Is the level at pin (6) 11 approx 0 dBm or is there > 1.0 V_{rms} at pin (6) 14 ?
Gain of output amplifier (6) to output too high!
0 dBm position of variable attenuator EL 601 defective!
Is the voltage at pin (12) 23 approx. 1 V_{pp} ?
P 1203 incorrectly adjusted (see Section 9.3.1.) or IC 1202 defective!
Reference generation (12) defective !
NO

RMS-4
Fault finding diagram
Level control circuit
Part 2

7.3.2.2. Level diagrams and oscillograms

The following section provides level diagrams for the frequency and level control circuits as a supplement to the fault finding diagrams in Section 7.3.2.1. These diagrams show the required levels and voltages for various settings of the RMS-4, if the unit is operating correctly.

The following test equipment is required for use of the level diagrams:

1 Digital voltmeter	e.g. 8000 A	Fluke
1 Millivoltmeter with VHF probe	e.g. 411 A with probe 11023 A	hp
1 Oscilloscope with 10:1 probe	e.g. PM 3240 with probe PM 9350	Philips

Level diagram of frequency control circuit
1st case: IF set to 70 and 140 MHz, no IF sweep

Settings on the RMS-4:

[4] (S 803) : Center frequency 70/140 MHz
[8] (S 902) : Sweep
[9] (S 903) : 70 MHz or 140 MHz
[17] (P 1305) : Fully anticlockwise
[34] (S 901) : Off (i.e. set to an unmarked position)

- Measure the voltages at the points specified in Table 7-2, using the digital voltmeter (see Figure 7-5 for the positions of the test points)

Test point	Voltage at point	
	[9] set to 70 MHz	[9] set to 140 MHz
(M1) to (M5), (M8)	0 V	0 V
(M6)	-3.9 V	-6.5 V
(M7)	-7.5 V	-11.5 V
	(see also Figure 7-4)	(see also Figure 7-4)

Table 7-2

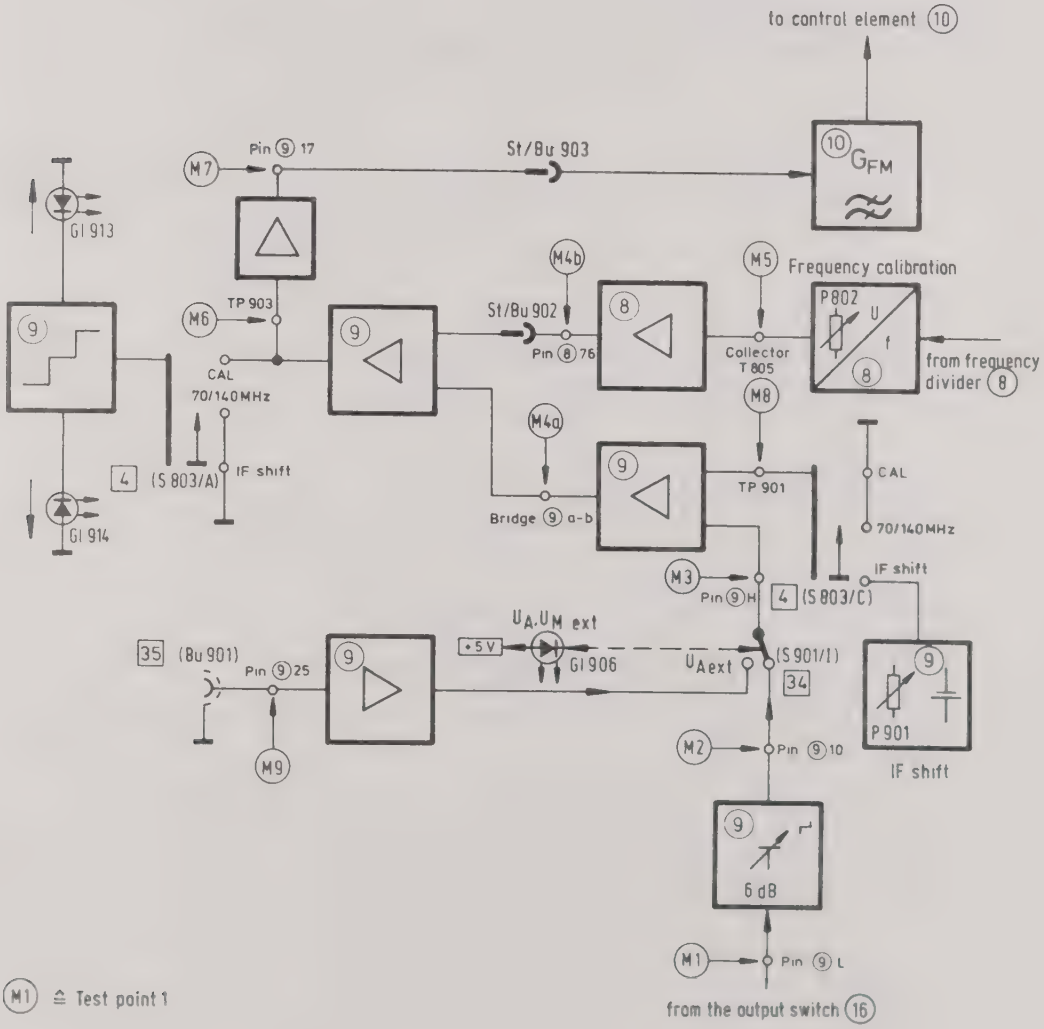


Figure 7-5 Level diagram of frequency control circuit, position of test points

2nd case: IF shifted by ± 25 or ± 50 MHz, no IF sweep

Settings on the RMS-4:

[3] (P 901) : Fully clockwise (≙ high IF) or fully anticlockwise (≙ low IF)
[4] (S 803) : IF shift
[8] (S 902) : Sweep
[9] (S 903) : 70 MHz or 140 MHz
[17] (P 1305) : Fully anticlockwise
[34] (S 901) : Off (i.e. set to an unmarked position)

- Measure the voltages at the test points specified in Table 7-3, using the digital voltmeter (see Figure 7-5 for the position of the test points)

	Voltage at test point			
	Set to 70 MHz		Set to 140 MHz	
Test point	[3] fully clockwise	[3] fully anti-clockwise	[3] fully clockwise	[3] fully anti-clockwise
(M1) to (M3)	0 V	0 V	0 V	0 V
(M4a), (M4b)	-8.1 V	+8.1 V	-8.1 V	+8.1 V
(M5)	-3.5 V	+3.5 V	-3.5 V	+3.5 V
(M6)	-6.5 V	-0.8 V	-9.2 V	-3.5 V
(M7)	-9.0 V	-5.7 V	-14.6 V	-8.7 V
	(See also Figure 7-4)	(See also Figure 7-4)	(See also Figure 7-4)	(See also Figure 7-4)
(M8)	+3.1 V	-3.1 V	+3.1 V	-3.1 V

Table 7-3

3rd case: IF set to 70 and 140 MHz, IF swept in the range ± 25 MHz or ± 50 MHz, respectively

Settings on the RMS-4:

[4] (S 803) : Center frequency 70/140 MHz
[7] (S 1301) : Off
[8] (S 902) : Sweep

[9] (S 903) : 70 MHz or 140 MHz
[17] (P 1305) : Fully clockwise
[18] (S 801) : 2 $\hat{\Delta}$F
[34] (S 901) : Off (i.e. set to an unmarked position)

- Measure at the test points shown in Table 7-4, using the oscilloscope. (See Figure 7-5 for positions of the test points).

Test point	Voltage at test point	
	[9] set to 70 MHz	[9] set to 140 MHz
(M1)	20 V_{pp}	20 V_{pp}
(M2), (M3)	10 V_{pp}	10 V_{pp}
(M4a), (M4b)	16 V_{pp}	16 V_{pp}
(M5)	7.0 V_{pp}	7.0 V_{pp}
(M6)	8 V_{pp}	8 V_{pp}
(M7)	4 V_{pp}	6 V_{pp}
(M8)	0 V	0 V

Table 7-4

4th case: IF set to 70 and 140 MHz;IF swept in the range $\pm$ 25 or $\pm$ 50 MHz, respectively; external input of U_A

Settings on the RMS-4:
[4] (S 803) : Center frequency 70/140 MHz
[8] (S 902) : Sweep
[9] (S 903) : 70 MHz or 140 MHz
[34] (S 901) : U_A, U_M ext.

- Inject an external sweep signal U_A with a value 5 V_{pp} (for 70 MHz IF) or 10 V_{pp} (for 140 MHz IF) at input [35] (Bu 901)
  If the sweep voltage generation circuit in the BF part of the RMS-4 is functioning correctly, this can be done as follows: establish a connection between output [14] (Bu 1605) on the front of the unit and

input [35] (Bu 901) on the rear of the unit; set the sweep frequency to 70 Hz with switch [20] (S 1302); adjust the sweep voltage U_A with potentiometer [17] (P 1305) to 2.5 V (with [9] (S 903) in position "70 MHz") or 5 V (with [9] (S 903) in the position "140 MHz"); potentiometer [16] (P 1501) fully anti-clockwise; pushbuttons [15] (S 1601) not depressed.

- Measure at the test points specified in Table 7-5, using the oscilloscope (see Figure 7-5 for the position of the test points).

Test point	Voltage at test point	
	[9] set to 70 MHz	[9] set to 140 MHz
(M1) , (M2)	Undefined	Undefined
(M3)	10 V_{pp}	10 V_{pp}
(M4a) , (M4b)	16 V_{pp}	16 V_{pp}
(M5)	7 V_{pp}	7 V_{pp}
(M6)	8 V_{pp}	8 V_{pp}
(M7)	4 V_{pp}	6 V_{pp}
(M8)	0 V	0 V
(M9)	5 V_{pp}	10 V_{pp}

Table 7-5

5th case: IF set to 70 and 140 MHz, sweep voltage U_A switched off internally.

Settings on the RMS-4:

[4] (S 803) : Center frequency 70/140 MHz
[9] (S 903) : 70 MHz or 140 MHz
[34] (S 901) : U_A, U_M ext.

- Measure the residual 500 kHz voltage as shown in Figure 7-6, with the oscillscope connected to test point (M4b)

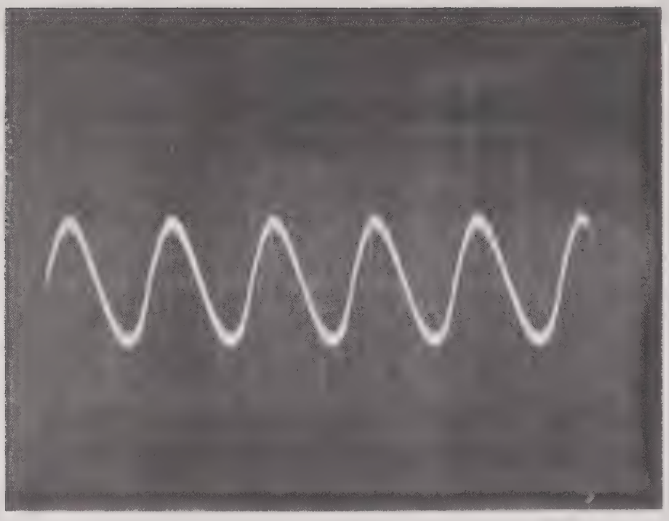


Figure 7-6 Residual 500 kHz voltage at pin (8) 76 or St/Bu 902
Vertical sensitivity: 10 mV/Div.
Horizontal deflection: 1 µs/Div.

- Measure the residual 500 kHz voltage as shown in Figure 7-7, with the oscilloscope connected to test point (M5) .

Figure 7-7 Residual 500 kHz voltage at the collector T 805
Vertical sensitivity: 0.2 V/Div.
Horizontal deflection: 0.5 µs/Div.

Level diagram of level control circuit

The level diagram for the level control circuit is divided into the sections amplifier chain (Figure 7-8) and reference generation and rectifier (Figure 7-9).

The specified levels and RMS voltages in the level diagram are to be checked with the millivoltmeter, the peak-to-peak voltages with the oscilloscope. Values which are marked in the level diagram with ⌟ are valid for the setting "-10 dBm" of potentiometer [2] (P 1201).

Settings on the MRS-4:

[2]	(P 1201)	:	0 dBm
[13]	(EL 601)	:	
[4]	(S 803)	:	Center frequency 70/140 MHz
[8]	(S 902)	:	Sweep
[9]	(S 903)	:	70 MHz
[16]	(P 1501)	:	Fully anticlockwise
[17]	(P 1305)	:	Fully anticlockwise

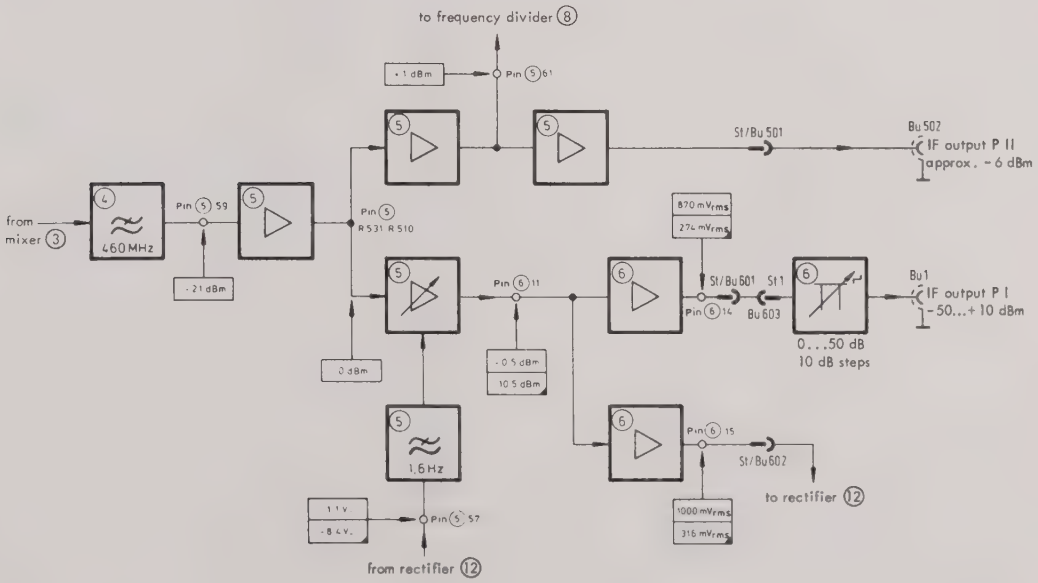


Figure 7-8 Level diagram, level control circuit, amplifier chain

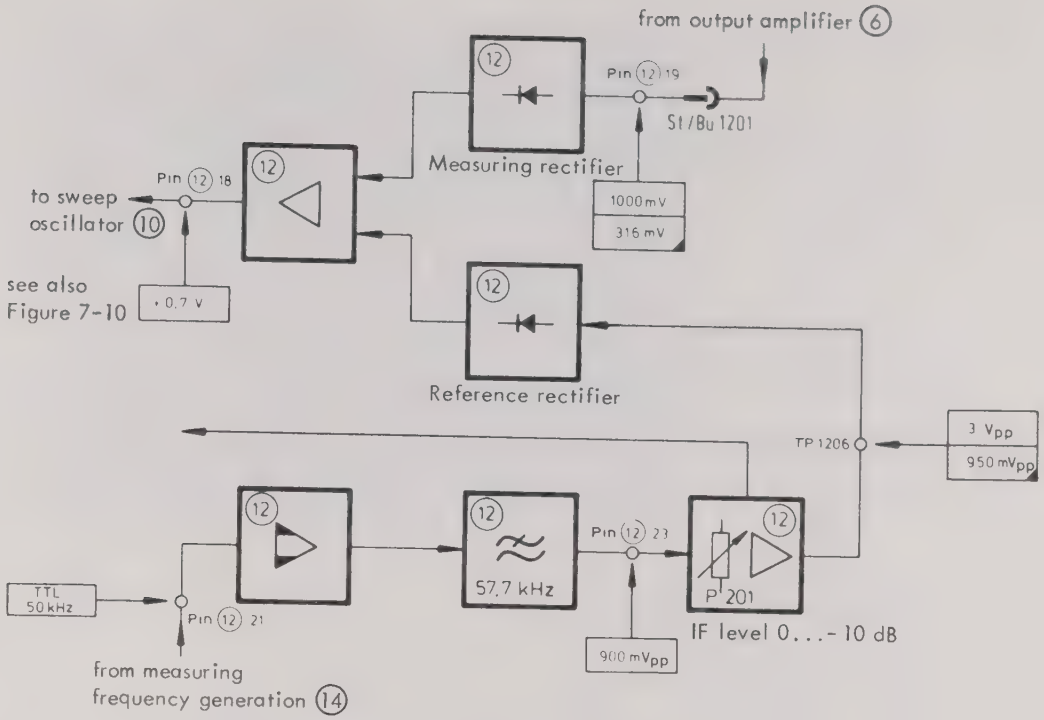


Figure 7-9 Level diagram, level control circuit, reference generation and rectifier

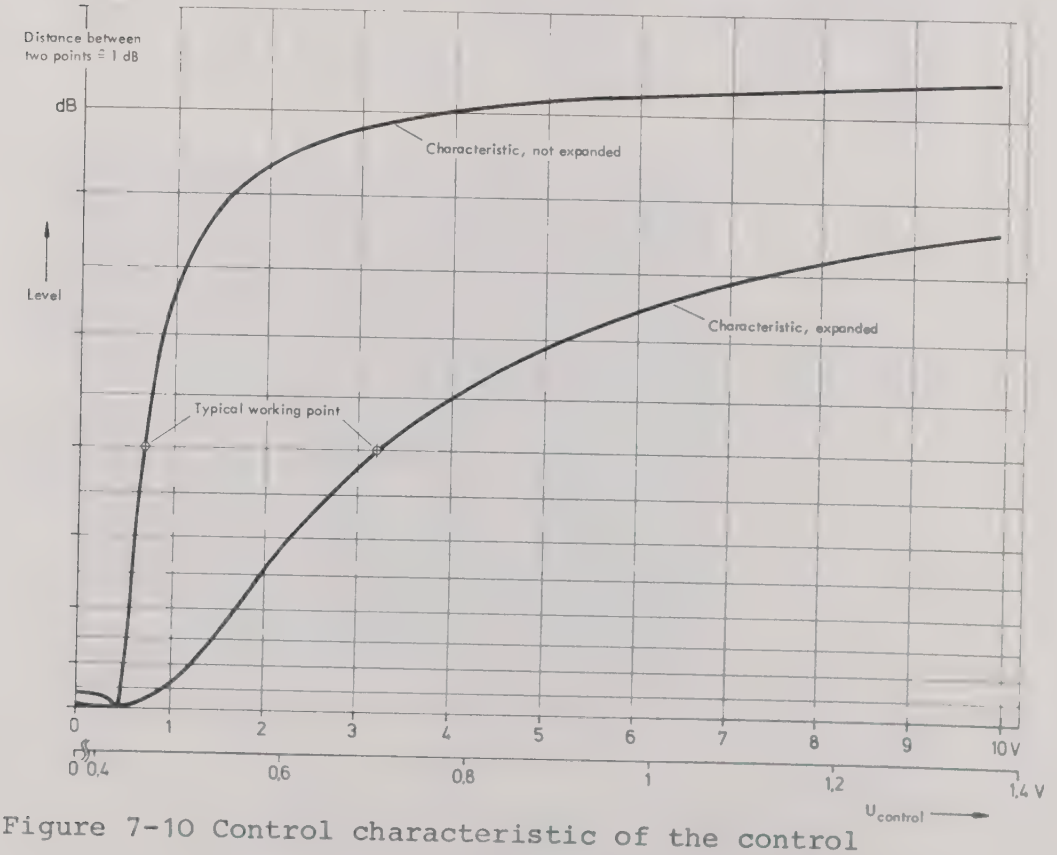


Figure 7-10 Control characteristic of the control element in the sweep oscillator (10)

7.3.2.3. Switch functions, IF section

Switch ☐ shown in circuit diagram ○	⑫	⑬	⑭	⑮	⑯	⑰	⑱	⑲	⑳	㉑	㉒	㉓	㉔	㉕	㉖	㉗	㉘	㉙
Switch ☐ controls	[illegible]	[illegible]	[illegible]	ref 901, R 920, IC 901, S 1, T 901, C 916, C 912	[illegible]	[illegible]	ref 1602, T 1601, T [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	S 801 II	[illegible]	S 901 I	B+ 1602, 1604 Pin 3	ref 1604
④ IF Bk 3 — IF shift	—	Shift voltage to control circuit	—	—	—	—												
④ IF Bk 3 — Center frequency 70; 140 MHz	—	—	—	—	—	—												
④ IF Bk 3 — CAL	500 kHz calibration frequency to discriminator	—	IC 904 connected as amplifier	Wideband function inactive	Output voltage of IC 905 is connected to comparator GI 913, GI 914	Sweep voltage disconnected from control circuit												
⑯ IF 902 — Sweep				—			—	—	—									
⑯ IF 902 — [illegible]				Wideband function active			U_M voltage disconnected from modulation oscillator	U_{SE} input connected to modulation oscillator	U_A disconnected from control circuit									
⑦ [illegible] — 140 MHz										Division factor increased to 280	—	Oscillator tuned circuit set to 140 MHz	Permits 2 ΔF via S 801 II					
⑦ [illegible] — [illegible]										—	Adjustment control circuit gain	—	Gain of IC 901 set to factor 2					
⑩ [illegible] — Δf														Lights for 140 MHz	2 Δf at 140 MHz Δf at 70 MHz			
⑩ [illegible] — Δf														—	—			
⑭ [illegible] — U_A, U_{Mext} [illegible]				Wideband function inactive			U_M voltage disconnected from modulation oscillator	U_{SE} input connected to modulation oscillator								Lights		
⑭ [illegible] — [illegible]				—			—	—								—	U_A ext control circuit	
S 903 on headset (BN 419.10) — [illegible]				Wideband [illegible] active		Sweep voltage disconnected from control circuit												12 V
S 903 on headset (BN 419.10) — Measurement				—		—												0 V
[illegible]																	[illegible] channel to modulation oscillator	—

Table 7-6

7.3.3. Fault finding in the BF section

Fault finding in the BF section is intended to determine whether the fault lies in the measuring voltage generation or sweep voltage generation.

Fault finding is carried out with fault finding diagrams and oscillograms. See Section 7.3.2.1. for the use of fault finding diagrams.

7.3.3.1. Fault finding diagrams

Test equipment required for fault finding:
1 Oscilloscope with 10:1 probe e.g. PM 3240 with probe 9350 Philips

Notes for the fault finding diagram "Measuring voltage generation"

1.

Settings on the RMS-4 before starting fault finding:

15 (S 1601) : not depressed
16 (P 1501) : fully clockwise
17 (P 1305) : fully anticlockwise
19 (S 1501) : explore all frequencies at each test point

2.

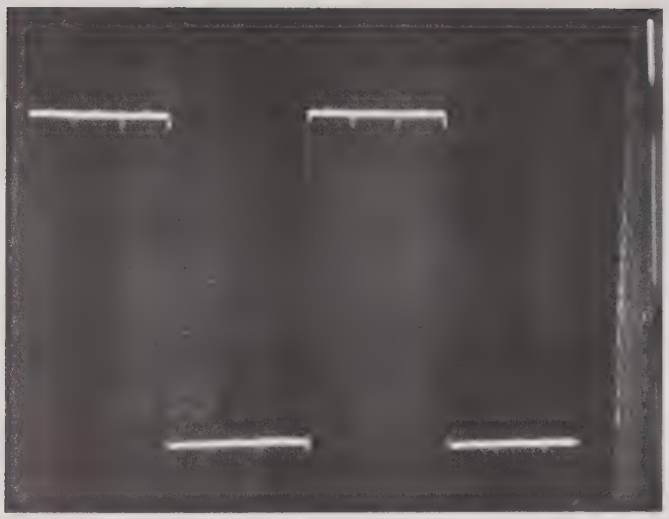


Figure 7-11 Measuring voltage U_M at pin (14) 71
f = 92.59 kHz, DC voltage of the center line +3.6 V
Vertical sensitivity: 0.2 V/Div.
Horizontal deflection: 2 µs/Div.

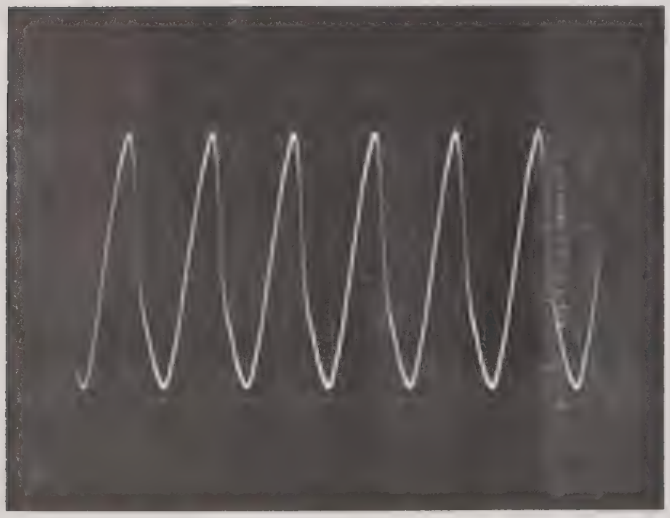


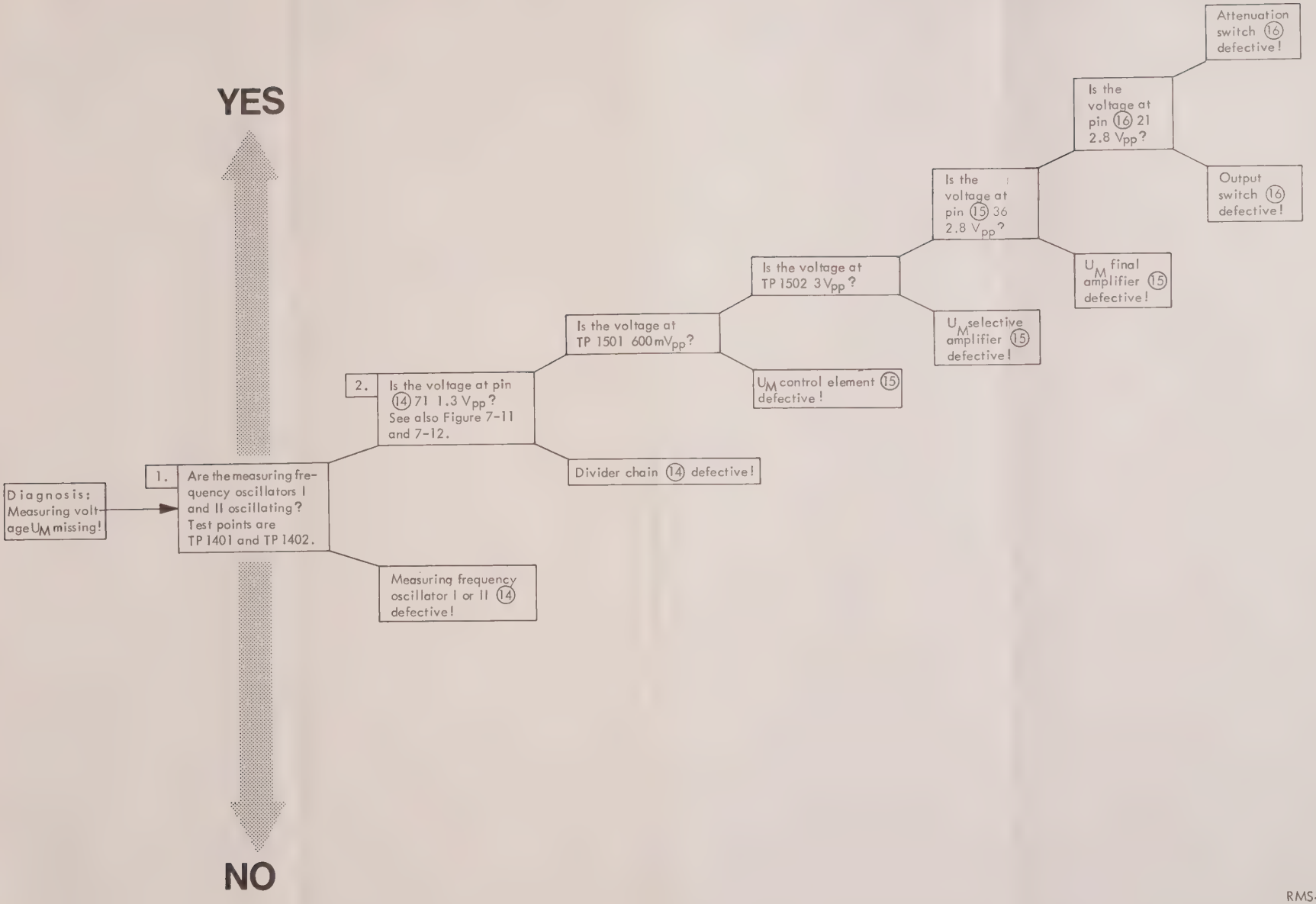
Figure 7-12 Measuring voltage U_M at pin (14) 71
f = 12.39 MHz, DC voltage of the center line +3.6 V
Vertical sensitivity: 0.2 V/Div.
Horizontal deflection: 50 ns/Div.

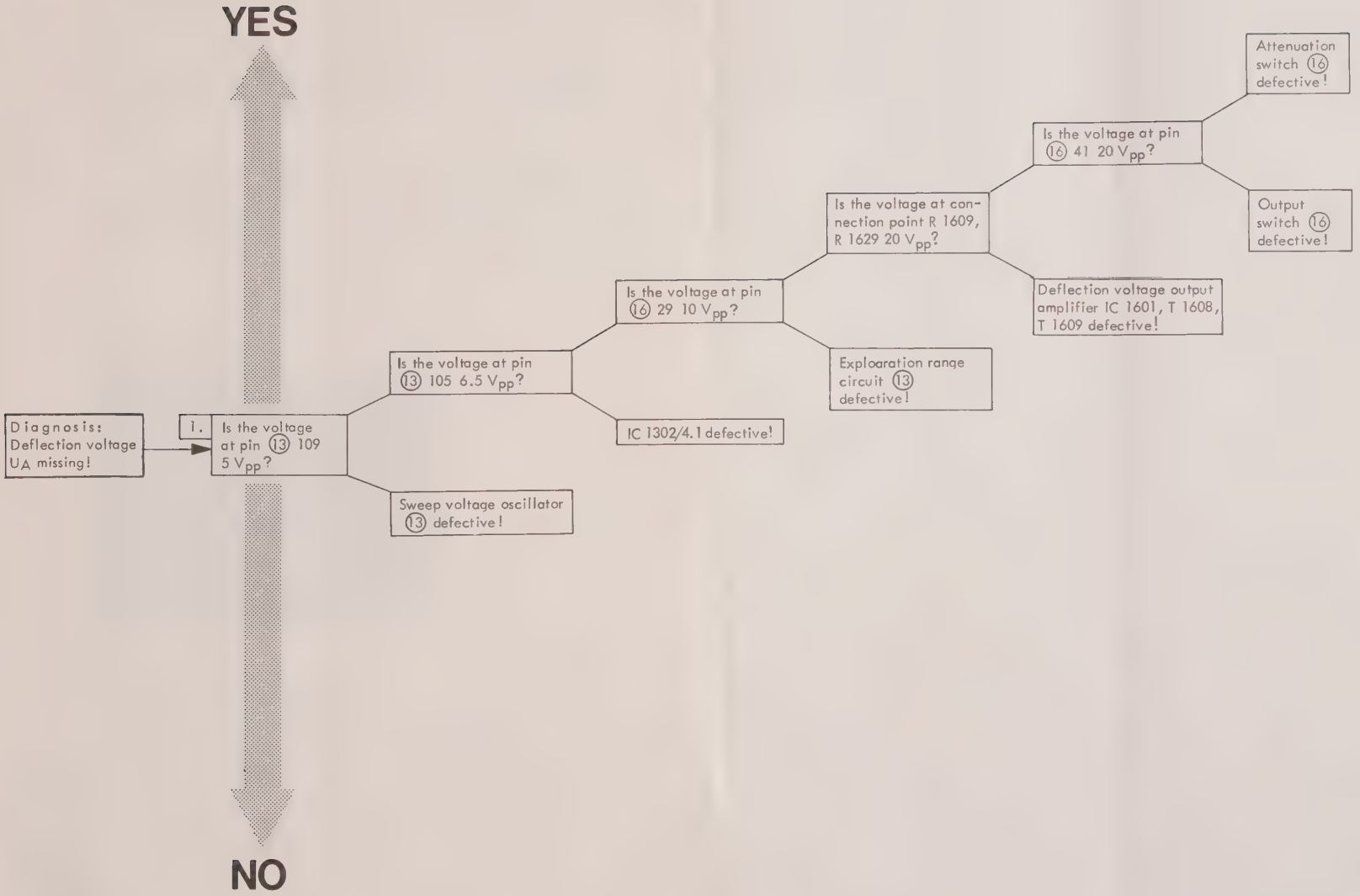
Notes for the fault finding diagram "Sweep voltage generation"

[1.]

Settings on the RMS-4 before starting fault finding:

[15] (S 1601) : not depressed
[16] (P 1501) : fully anticlockwise
[17] (P 1305) : fully clockwise
[7] (S 1301) : off


YES
NO
Diagnosis: Measuring voltage U_M missing!
1. Are the measuring frequency oscillators I and II oscillating? Test points are TP 1401 and TP 1402.
Measuring frequency oscillator I or II (14) defective!
2. Is the voltage at pin (14) 71 1.3 V_{pp}? See also Figure 7-11 and 7-12.
Divider chain (14) defective!
Is the voltage at TP 1501 600 mV_{pp}?
U_M control element (15) defective!
Is the voltage at TP 1502 3 V_{pp}?
U_M selective amplifier (15) defective!
Is the voltage at pin (15) 36 2.8 V_{pp}?
U_M final amplifier (15) defective!
Is the voltage at pin (16) 21 2.8 V_{pp}?
Output switch (16) defective!
Attenuation switch (16) defective!


YES
NO
Diagnosis: Deflection voltage UA missing!
1.
Is the voltage at pin (13) 109 5 Vpp?
Sweep voltage oscillator (13) defective!
Is the voltage at pin (13) 105 6.5 Vpp?
IC 1302/4.1 defective!
Is the voltage at pin (16) 29 10 Vpp?
Exploaration range circuit (13) defective!
Is the voltage at connection point R 1609, R 1629 20 Vpp?
Deflection voltage output amplifier IC 1601, T 1608, T 1609 defective!
Is the voltage at pin (16) 41 20 Vpp?
Output switch (16) defective!
Attenuation switch (16) defective!

RM
Fault finding diag
Deflection voltgae genera

7.3.3.2. Fault finding in the case of defects in the blanking gap

The blanking gap is used for recognition and setting of the phase relationships of BF distortion results in the receive section RME-4.

When pushbutton [21] (S 1303) is depressed, a gap pulse temporarily reduces the measuring voltage in the assembly U_M amplifier, U_M control element (15). This state is shown by the oscillogram in Figure 7-13.

The sum signal $\hat{U}_A + U_M$ with blanking gap at output [14] (Bu 1605) is shown in Figure 7-14.

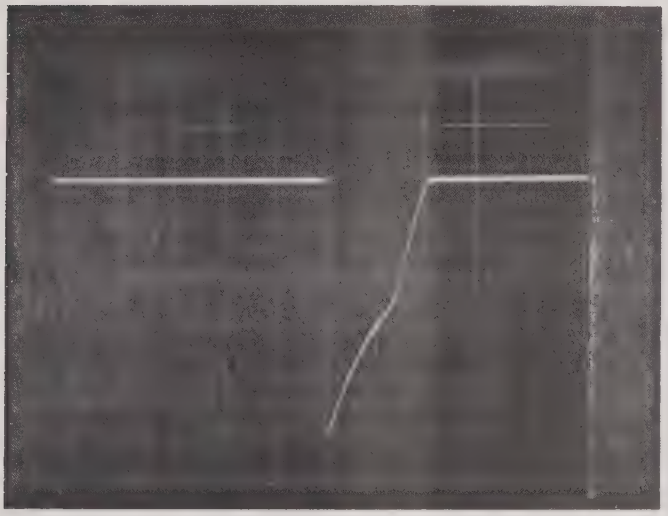


Figure 7-13 Gap pulse at pin (15) 63
Horizontal line: -3 V
Vertical sensitivity: 0.2 V/Div.
Horizontal deflection: 0.2 ms/Div.

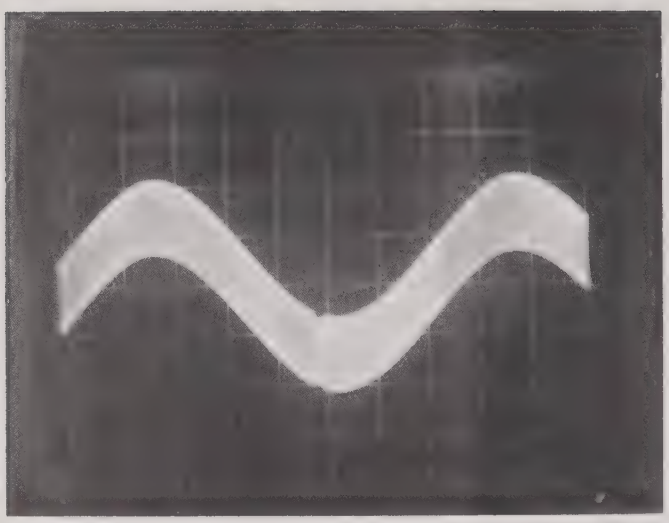


Figure 7-14 Sum signal $\hat{U}_A + U_M$ with blanking gap at output [14] (Bu 1605) Sweep frequency f_A = 70 Hz

7.3.3.3. Switch funktions in BF section

Switch	Switch [...] shown in circuit diagram (...)	Acts on
[19] (S 1501) 0.093 (0.083) MHz	⑬, ⑭, ⑮	Pins ⑬ 99, ⑭ 74, ⑮ 52
[19] (S 1501) 0.277 (0.250) MHz	⑬, ⑭, ⑮	Pins ⑬ 98, ⑭ 73, ⑮ 50
[19] (S 1501) 0.555 (0.500) MHz	⑬, ⑭, ⑮	Pins ⑬ 97, ⑭ 75, ⑮ 48
[19] (S 1501) 2.4 MHz	⑬, ⑭, ⑮	Pins ⑬ 96, ⑭ 72, ⑮ 46
[19] (S 1501) f_{sc}	⑬, ⑭, ⑮	Pins ⑬ 95, ⑭ 76, ⑮ 44
[19] (S 1501) 5.6 MHz	⑬, ⑭, ⑮	Pins ⑬ 93, ⑭ 77, ⑮ 42
[19] (S 1501) 8.2 MHz	⑬, ⑭, ⑮	Pins ⑬ 94, ⑭ 78, ⑮ 39
[19] (S 1501) 12.39 MHz The specified allocations are valid only with the color subcarrier fitted	⑬, ⑭, ⑮	Pins ⑬ 110, ⑭ 79, ⑮ 37
[7] (S 1301) On	⑬	Gl 1308 lights if $F_M > \hat{\Delta F_A}$ Gl 1306 lights
[7] (S 1301) Explored range	⑬	Pin ⑬ 90: U_A reduction by a short-circuit not possible
[7] (S 1301) Off	⑬	
[20] (S 1302) 70 Hz	⑬	rel 1301: frequency switching at IC 1301 rel 1302: switching of the absolute level calibration
[20] (S 1302) 18 Hz	⑬	
[21] (S 1303) Gap	⑬	Causes square-wave pulses to be applied to U_M control element

Table 7-6a

7.4. Disassembly work

Note: Before disassembling the unit, switch off the unit and remove the mains plug from the outlet socket!

7.4.1. Removal of the unit chassis

Removal of the unit chassis from the complete unit is carried out as follows:

- Place the unit on the bench in its normal position
- Remove the cover by loosening the 6 hexagon head cap screws with the aid of the enclosed wrench
- Disconnect the cable connections between the equipment chassis and the power supply unit (8-pole AF plug connectors St 1/Bu 101 and St 2/Bu 102)
- Carefully lift the chassis upwards out of the unit.

Note: Before lifting out the chassis, remove the spare fuses from the case cutout on the rear.

IF repair of the unit was preceded by fault finding, it can be assumed that the disassembly state and the position of the unit corresponds to Section 7.1. The unit chassis is practically free. It is only necessary to disconnect the cable connections between the unit chassis and the power supply unit to permit complete disconnection of the chassis from the right sidewall. After this, the chassis can be removed from the right sidewall by sliding sideways in the guide slots. See the above note.

7.4.2. Removal of the power supply unit

The power supply unit forms a single unit with the right sidewall. Removal is carried out as follows:

- Place the equipment on the left sidewall
- Loosen the screw connections between the right sidewall and the cover and the baseplate
- Place the unit in its normal position and completely remove the cover
- Disconnect the cable connections between the power supply unit and the equipment chassis (8-pole AF plug connectors St 1/Bu 101 and St 2/Bu 102).
- Lift the equipment chassis out of the unit until the right sidewall can be removed to the side together with the power supply. See the note in Section 7.4.1.

7.4.3. Removal and fitting of knobs

Removal:
- Lift off the cover of the knob with a knife
- Loosen the clamping cone with a socket wrench (SW 12) or screwdrive (depending on the type of knob)
- Pull the knob from the shaft; if the clamping cone does not release itself automatically, tap the front of the knob with the screwdriver

Fitting:
Potentiometer [2] (P 1201):
- Fit the knob so that the 0 dB mark coincides with the line on the front panel with the potentiometer turned fully clockwise.

Switch [13] (EL 601):
- Fit the knob so that the +10 dBm mark coincides with the line on the front panel when the variable attenuator is set fully clockwise.

Potentiometer [16] (P 1501):
- Set the potentiometer so that the scale mark to the left of +5 dBm on the dBm scale coincides with the line on the front panel
- Then fit the knob so that the mark on the knob coincides with the 500 mV position.

Potentiometer [17] (P 1305):

- Required test equipment: 1 Digital voltemeter (AC) e.g. Fluke 8000 A
- Turn the potentiometer [16] (P 1501) fully anticlockwise
- Turn potentiometer [17] (P 1305) fully clockwise
- Series B units and later: Set switch [20] (S 1302) to position "70 Hz"
- Measure the voltage at socket [16] (Bu 1605)
- Adjust potentiometer [17] (P 1305) such that the maximum output voltage at socket [16] (Bu 1605) is reduced by 0.2 %.
- In this position of the potentiometer, fit the knob so that the mark on the knob coincides with the 5 V mark on the scale.

7.4.4. Removal of printed circuits

For screening reasons, the printed circuits are installed in enclosed metallized plastic containers. For removal of a printed circuit, the cover of the container must first be lifted off with the plastic loop provided for this purpose.

After the connecting wires have been unsoldered and all plug connections disconnected from the printed circuit, remove all Phillips-head screws which hold the printed circuit board in position. After this, the printed circuit can be lifted out of the container - most of the printed circuit boards are equipped with a special card puller for this purpose.

7.4.5. Removal of the upper carrier board (board [696-M...])

For removal of the upper carrier board, the cover of the unit must be removed as described in Section 7.4.1.

Then proceed as follows:

- Disconnect the HF connection between the variable attenuator and plug St 601 on the carrier board
- Unsolder the connections on potentiometer [5] (P 802) and loosen the cable clamp
- Release the retainers on the 2 x 10-pole plug strip (designation 00-7015.03) and pull out the socket strip
- Loosen the 10 Phillips-head screws which hold the carrier board on the frame
- Lift up the carrier board and disconnect the Subminax connectors between the upper and lower carrier board (board [696-S...])
- Lift out the carrier board

7.4.6. Removal of the lower carrier board (board [696-K...])

The baseplate of the unit must be removed for removal of the lower carrier board. To do this, first place the unit on its cover and remove the six hexagon head cap screws which connect the baseplate to the sidewalls, using the enclosed hexagonal wrench.

Then proceed as follows:

- Remove the board ([696-H...]) (3 Phillips-head screws)
- Disconnect the Subminax connector from plug St 1601
- Loosen the remove the 10 Phillips-head screws with which the carrier board is screwed to the frame
- Lift the loosened carrier board, release the retainers on the 2 x 15-pole plug strip (designation 00-7015.05) and pull it out of the socket strip; also disconnect the Subminax connectors between the upper and lower carrier boards and board [696-S...]
- Lift out the carrier board.

7.4.7. Partial removal of the front panel

Partial removal of the front panel is necessary only if the variable attenuator is to be removed (see also Section 7.4.8.). All other controls on the front panel can be removed while the front panel is still connected to the chassis.

- Remove the unit chassis as described in Section 7.4.1.
- Remove the knobs and the adapters of the universal sockets Versacon® 9 from the front panel
- Remove the printed cover board (4 oval head screws)
- Disconnect the HF connection between the variable attenuator and plug St 601 on the output amplifier (6)
- If the optional feature "IF calibration generator" is fitted: remove the Subminax connector from socket [12] (Bu 1801)
- Remove the front panel from the unit chassis (4 countersunk Phillips-head screws)
- The remaining electrical connections to the controls on the front panel are sufficiently long to permit the front panel to be lifted away from the unit chassis such that the variable attenuator can be removed (see also Section 7.4.8.).

7.4.8. Removal of the variable attenuator [13] (EL 601)

- Partial remove the front panel as described in Section 7.4.7.
- Unscrew socket [1] (Bu 1) from the front panel (2 countersunk head screws)
- Remove the variable attenuator from the front panel (4 countersunk Phillips head screws)
- Lift out the variable attenuator between the front panel and the unit chassis

7.4.9. Removal and soldering of chip components

Required tools:
Temperature-controlled soldering iron with forked tip, e.g. Weller-Magnastat (50 to 80 W), with soldering tip group 5 (up to 260° C) or group 6 (up to 310° C) or adjustable soldering iron Zeva G 5 T (65 W), setting 280° C.

Solder Type C 3 (1 mm Ø) with 1.5 % flux is to be used.

When unsoldering and soldering in such components, the maximum permissible temperature of the soldering point is 240° C. This temperature is not exceeded if the soldering time is kept as short as possible (maximum 3 x).

Before soldering in the component, tin the soldering position on the BS side of the printed circuit board. The component is then placed with its connection surfaces on the soldering position. Both soldering points on the printed circuit are then heated simultaneously with the forked soldering tip; the soldering tip must not touch the component. If necessary, the component can be held in position with a small piece of wood while soldering. If it is necessary to solder in two chips which lie alongside each other, then allow the first chip to cool for a short time before soldering in the second chip. Chip capacitors may be held with metal tweezers only across the contact surfaces.

8. CHECKING IMPORTANT TECHNICAL DATA

The following section describes methods which permit the most important characteristic values of the equipment to be checked. Wherever possible, commercially available test equipment is suggested.

Unless otherwise specified, the tests should be carried out within the nominal operating range for temperature and mains voltage.

If a warming up period is specified in the technical data, then the tests should be started only after this period.

Checking of the most important data is intended to determine whether the indication of a measured value lies within the guaranteed error limit. Successful checking without restrictions is possible only if the intrinsic errors of the test configuration used are negligible.

Otherwise, the following rule applies:
if $\pm$ e is specified as the guaranteed error limits for the unit being tested and if the error of the test configuration used is $\pm$ m, then

> a value outside the limits $\pm$ (e + m) indicates that the guaranteed error limits have certainly been exceeded;
>
> a value within the limits $\pm$ (e - m) indicates that the error limits are certainly maintained.

The value e is specified in the instructions for each test. The value m depends on the test equipment used and must therefore generally be determined from case to case. The testing instructions mention the value of

m only if the prescribed test equipment permits no variation or if special conditions are to be observed.

For systematic checking of the data, the tests should be carried out in the order specified here.

Adjustment of the unit being tested should be carried out only if a value outside the limits $\pm$ (e + m) is determined. The necessary adjustment operations are described in Chapter 9.

Note:

Some of the important technical data of the RMS-4 are checked by means of a back-to-back measurement between the RMS-4 and the RME-4. However, it is not possible to determine the specific error of one unit with this method, but only the overall error of the combination of units. The back-to-back measurment is used either because it is not possible to prove the technical data in another manner (applies to: intrinsic distortion, intrinsic noise of the distortion measurement results, intrinsic frequency response, noise characteristics, and modulation frequency response) or in order to keep the amount of test equipment required within reasonable limits (applies to: effective deviation and sweep width).

All back-to-back measurements are described in the servicing instructions for the RME-4.

8.1. Error limits of the frequency

8.1.1. IF center frequencies 70 and 140 MHz

Required test equipment:
1 Digital frequency meter (up to 2 MHz) e.g. FZ-4 W&G

Equipment settings:
RMS-4: [8] (S 902) : Wideband
[9] (S 903) : 70 MHz
FZ-4: Measuring time 0.1 s

- Connect the digital frequency meter to socket [31] (Bu 802) on the rear of the RMS-4 (Output for 0.01 x IF)
- Set switch [4] (S 803) to "CAL" and adjust potentiometer [5] (P 802) so that LEDs Gl 913 and Gl 914 are both off.
- Turn switch [4] (S 803) to "Center frequency" and read off the frequency from the digital frequency meter
  Switch [9] (S 903) set to 70 MHz:
  700 kHz ± 0.5 kHz (Error limits e)
  Switch [9] (S 903) set to 140 MHz:
  1400 kHz ± 1.0 kHz (Error limits e)
- If switch [4] (S 803) is turned to position "IF offset", the range of the IF offset (± 25 or ± 50 MHz) can be checked:
  frequency variation indicated on the digital frequency meter is ± 250 or ± 500 kHz.

8.1.2. Measuring frequencies

Required test equipment:
1 Digital frequency meter (up to 20 MHz) e.g. FZ-4 W&G

Equipment settings:
RMS-4: [15] (S 1601) : not depressed
[16] (P 1501) : 500 mV (fully clockwise)
[17] (P 1305) : 0 V (fully anticlockwise)
FZ-4: Measuring time according to measuring frequency

- Connect the digital frequency meter to socket [14] (Bu 1605)
- Check all measuring frequencies with switch [19] (S 1501) in its various positions

Measuring frequency/MHz		Display/kHz		Error limits $e \hat{=} \pm 2.5 \cdot 10^{-5} f_M$	
Series I	Series II	Series I	Series II	Series I	Series II
0.093	0.083	92.592	83.333	± 1.8 Hz	± 1.6 Hz
0.277	0.250	277.777	250.000	± 5.5 Hz	± 5 Hz
0.555	0.500	555.555	500,000	± 11 Hz	± 10 Hz
2.4		2400.00		± 48 Hz	
5.6		5600.00		± 112 Hz	
8,2		8200.00		± 164 Hz	
12.39		12390,0		± 248 Hz	

Table 8-1

8.1.3. Sweep frequencies

Required test equipment:
1 Digital frequency meter e.g. FZ-4 W&G

Equipment settings:
RMS-4: [15] (S 1601) : 20 dB
[16] (P 1501) : 0 V (fully anticlockwise)
[17] (P 1305) : Approx. 1 V
[7] (S 1301) : off
FZ-4 Measuring time 10 s

- Connect the digital frequency meter to socket [14] (Bu 1605)
- Check the sweep frequencies with switch [20] (S 1302) in both positions
  Switch [20] (S 1302) set to 70 Hz:
  70 Hz $\pm$ 1.4 Hz (Error limit e)
  Switch [20] (S 1302) set to 18 Hz:
  18 Hz $\pm$ 0.36 Hz (Error limit e)

8.2. Error limits of the selected level

8.2.1. IF output level P_I

Required test equipment:
1 Calibrated level meter with probe e.g. EPM-1 with TK-10 W&G
1 Attenuator 9.03 dB Accessory for EPM-1

Equipment settings:
RMS-4: [2] (P 1201) : 0 dB
[13] (EL 601) : 0 dBm
[4] (S 803) : Center frequency 70/140 MHz
EPM-1: Measuring range ± 0.2 dBm, calibrated with 0 dBm, R_i = 75 Ohm

Check at P_I = 0 dBm:
- Connect the probe of the calibrated level meter to socket [1] (Bu 1) of the RMS-4
- Read off the deviation from 0 dBm on the calibrated level meter in both positions of switch [9] (S 903), i.e. with an IF of 70 and 140 MHz
  Error limits e: ± 0.2 dB

Check of the frequency response at P_I = 0 dBm:
- Set switch [4] (S 803) on the RMS-4 to the position "IF offset" and set switch [9] (S 903) to 70 MHz
- Slowly turn potentiometer [3] (P 901) from -25 to +25 MHz and observe the variation of the indication on the calibrated level meter
  Frequency reponse referred to the center value ± 0.15 dB (Error limit e)
- Set switch [9] (S 903) to 140 MHz and repeat the above measurement.
  Frequency response referred to the center value + 0.3 dB (Error limit e)

Check at P_I = +10 dBm:

- Change the level setting on the RMS-4: [2] (P 1201) to -1.0 dB and [13] (EL 601) to +10 dBm; set switch [4] (S 803) to center frequency 70/140 MHz
- Switch the calibrated level meter to the measuring range ± 1 dBm; connect the 9.03 dB attenuator and calibrate with 0 dB, R_i = 75 Ohm
- Connect the probe of the calibrated level meter, with the attenuator connected, to socket [1] (Bu 1) of the RMS-4
- Read off the deviation from -0.03 dBm on the calibrated level meter in both positions of switch [9] (S 903), i.e. with an IF of 70 and 140 MHz
  Error limit e: ± 0.5 dB

8.2.2. Measuring voltage U_M

Required test equipment:

1 Calibrated level meter with probe: e.g. EPM-1 with TK-10 W&G

Equipment settings:

RMS-4: [15] (S 1601) : not depressed
[16] (P 1501) : 0 dBm ($\hat{=} V_{rms}$ = 274 mV)
[17] (P 1305) : 0 V (fully anticlockwise)

EPM-1: Measuring range ± 1 dBm, calibrated with 0 dBm, R_i = 75 Ohm

- Connect the probe of the calibrated level meter to socket [14] (Bu 1605)
- Measure the level deviation from 0 dBm for all frequencies (switch [19] (S 1501)) with the calibrated level meter
  Error limits e of the level divations: ± 0.7 dB
  (this corresponds to the error limits ± 15 mV ± 0.03 U_M)

8.2.3. Deflection voltage $\hat{U}_A$

Required test equipment:

1 Digital voltmeter	e.g. 8600 A	Fluke
2 DC power supplies	e.g. GS-2	W&G
1 Oscilloscope	e.g. PM 3240	Philips
1 $\hat{U}_A$ calibration device	as described in Figure 9-45 and Table 9-5	

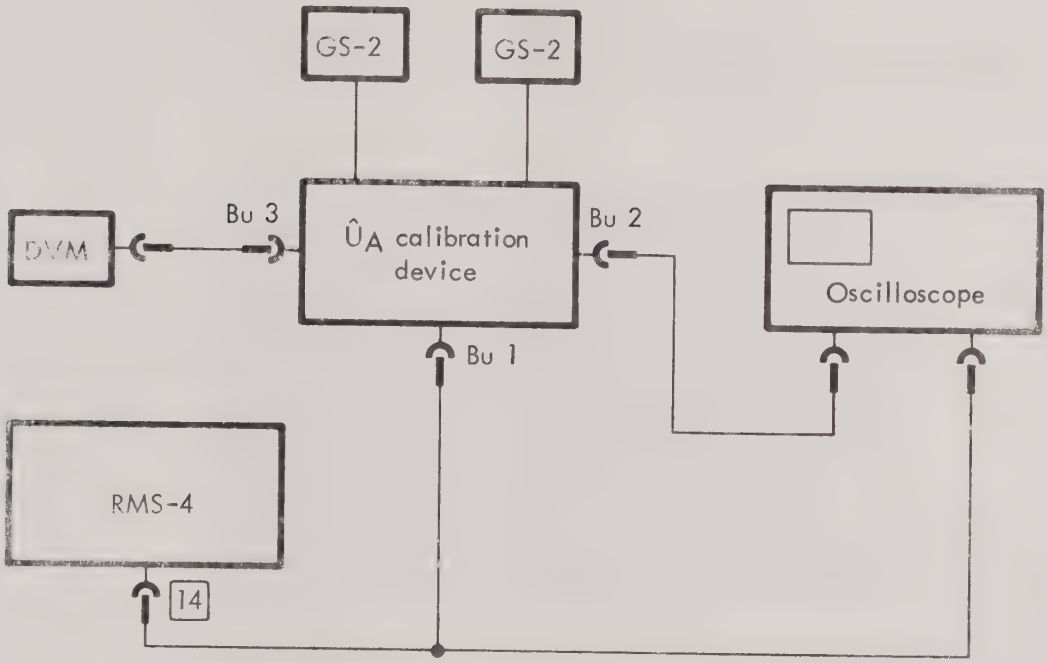


Figure 8-1 Test configuration for Section 8.2.3

Equipment settings:

RMS-4:

[4]	(S 803) :	Center frequency 70/140 MHz
[7]	(S 1301):	off
[15]	(S 1601):	not depressed
[16]	(P 1501):	0 V (fully anticlockwise)
[17]	(P 1305):	5 V (scale mark)
[20]	(S 1302):	70 Hz

Oscilloscope: DC coupling, Y sensitivity 50 mV/Div. X sensitivity 2 V/Div.

Power supplies: $\pm$ 12 V $\pm$ 1 %

$\hat{U}_A$ calibration device: adjust potentiometer P 4 for a voltage of +5 V $\pm$ 5 mV (indicated on DVM)

- Read off the distance A between the positive and negative peaks of the deflection voltage on the oscilloscope (see Figure 8-2).
  Error limits (e): 200 mV (= 4 divisions on the screen)
  (This corresponds to the error limits +50 mV +0.03 U_A)
- Repeat the measurement at f_A = 18 Hz; error limits as above.

Note: If the oscilloscope used is not capable of handling large signals, measuring errors may occur

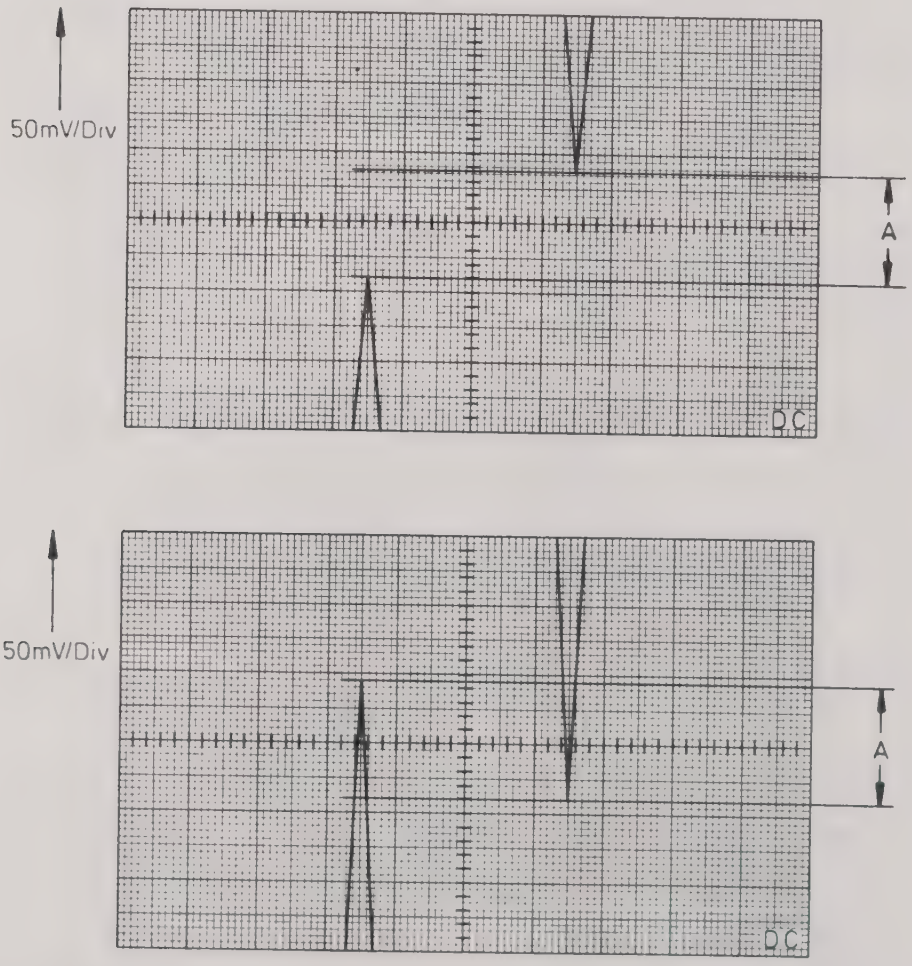


Figure 8-2

8.2.4. Explored range $\Delta \hat{f}_A$

Required test equipment and test configuration as in Section 8.2.3.

Equipment settings:

RMS-4:
- [4] (S 803) : Center frequency 70/140 MHz
- [6] (P 1303): ± 30 MHz
- [7] (S 1301): off
- [15] (S 1601): not depressed
- [16] (P 1501): 0 V (fully anticlockwise)
- [17] (P 1305): 5 V (scale mark)
- [20] (S 1302): 70 Hz

Oscilloscope and power supplies: as in Section 8.2.3.

Setting up the reference point:
- Adjust potentiometer P 4 on the $\hat{U}_A$ calibration device for a voltage of +4.800 V (indicated on the DVM)
- On the oscilloscope, adjust potentiometer [17] (P 1305) until the distance A (see Figure 8-2) is zero

Measurement:
- Switch on the explored range switch [7] (S 1301)
- Selection the built-in measuring frequencies one after another with switch [19] (S 1501); compensate for the reduced deflection voltage with potentiometer P 4 in each case such that the gap A on the screen of the oscilloscope is again zero. Read off the compensation voltage on the DVM and compare it with the required value shown in Table 8-2.

Note: The required values are calculated with the formula $U_{P4} = 4.8\ V \left(1 - \frac{f_M}{30\ MHz}\right)$

The error limits correspond to the value:
$\pm$ 350 kHz $\pm$ 0.03 . f_M

f_M [19] [MHz]	Required values [V] (=Up4)	Error limits (e) [mV]
0.083	4.787	± 70
0.093	4.785	± 71
0.25	4.760	± 72
0.277	4.756	± 72
0.5	4.720	± 73
0.555	4.711	± 73
2.4	4.416	± 84
3.58	4.227	± 91
4.43	4.091	± 97
5.6	3.904	± 104
8.2	3.488	± 119
12.39	2.818	± 144

Table 8-2

8.3. Harmonic ratio

8.3.1. Harmonic ratio at IF output P_I

Required test equipment:

1 Spectrum analyzer e.g. 8558B/182T hp

1 Matching element 75 Ohm ⟶ 50 Ohm

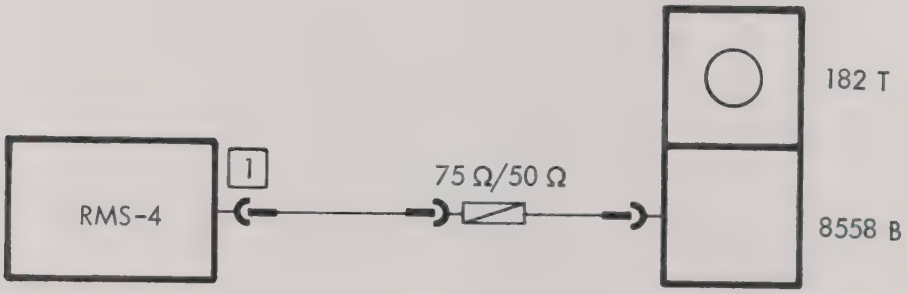


Figure 8-3 Test configuration for Section 8.3.1.

Equipment settings:

RMS-4: [2] (P 1201) : 0 dB
[13] (EL 601) : 0 dBm
[4] (S 803) : IF offset
[8] (S 902) : Wideband

8558 B: Ref. Level approx. -8 dBm, 10 dB/Div.
Frequency start 0 MHz
100 MHz/Div, 20 ms/Div.

- Adjust the Ref. Lev. on the spectrum analyzer such that the basic frequency reaches the 0 dB line on the graticule
- Tune through the complete frequency range with potentiometer [3] (P 901) and switch [9] (S 903) and read off a_{k2} and a_{k3} from the spectrum analyzer.
  Harmonic ratios a_{k2} and a_{k3}: $\geq$ 30 dB (Error limit e)
- Change the level setting of the RMS-4: [2] (P 1201) to -10 dB and [13] (EL 601) to +10 dBm
- Repeat the measurement
  Harmonic ratios a_{k2} and a_{k3}: $\geq$ 30 dB (Error limit e)

8.3.2. Harmonic ratio of the measuring voltage U_M

Required test equipment:

1 Spectrum analyzer e.g. 8558 B/182 T hp
1 Matching element 75 Ohm $\longrightarrow$ 50 Ohm

Test configuration as in Figure 8-3, but with the spectrum analyzer connected to socket [14] (Bu 1605) of the RMS-4.

Equipment settings:

RMS-4: [15] (S 1601) : Not depressed
[16] (P 1501) : 500 mV (fully clockwise)
[19] (S 1501) : 12.39 MHz

8558 B: Ref. level approx. -2.5 dB, 10 dB/Div.
Frequency start 0 MHz
10 MHz/Div., 10 ms/Div.

- Adjust the Rev. Level on the spectrum analyzer so that the basic frequency reaches the 0 dB line on the graticule.
  Read off the harmonic ratios a_{k2} and a_{k3} on the spectrum analyzer.
  Harmonic ratios a_{k2} and a_{k3}: $\geq$ 30 dB (Error limit e)
- The other measuring frequencies can be checked in the same manner.

8.4. Return loss

8.4.1. Return loss of the IF connections

Required test equipment:

1 Radio link measuring setup RM-4	W&G
1 Return loss measuring bridge RFZ-4	W&G

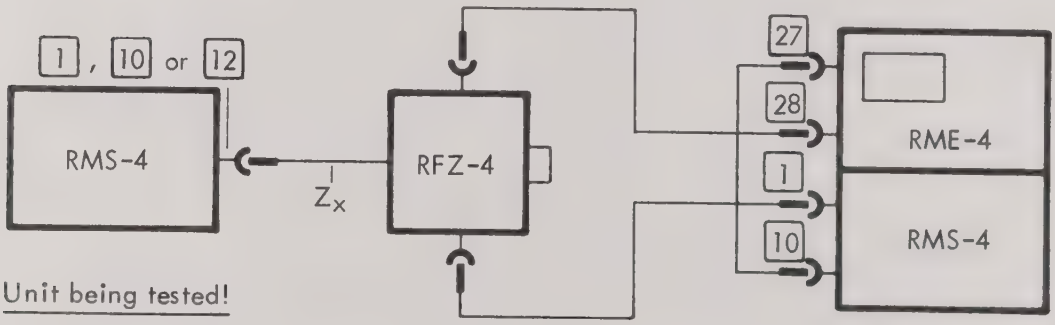


Figure 8-4 Test configuration for Section 8.4.1.

Equipment settings:

RMS-4 (Unit being tested) :

2	(P 1201)	: -10 dB
13	(EL 601)	: +10 dBm
9	(S 903)	: 140 MHz
16	(P 1501)	: Fully anti-clockwise
17	(P 1305)	: Fully anti-clockwise

RMS-4 (Test setup):	[2]	(P 1201) :	0 dB
	[13]	(EL 601) :	-20 dBm
	[7]	(S 1301) :	Off
	[8]	(S 902) :	Sweep
	[9]	(S 903) :	70 MHz
	[16]	(P 1501) :	Fully anticlockwise
	[17]	(P 1305) :	25 MHz (fully clockwise)
	[18]	(S 801) :	2 $\Delta\hat{F}$
RME-4 (Test setup):	[29]	(S 1601) :	Input IF
	[31]	(EL 701) :	0 dBm
	[36]	(S 1401) :	Tracking
	[27]	(S 1402) :	70 MHz
	[9]	(S 2203) :	ΔP_{II} depressed
	[14]	(P 2203) :	Fully clockwise
	[15]	(S 1503) :	Not depressed

Calibration:

- Connect the measuring bridge RFZ-4 without the unit to be tested.
- Adjust potentiometer [8] (P 2201) on the RME-4 so that the indication lies on the -30 dB graticule line: this reference line corresponds to a return loss a_r of 30 dB during subsequent measurement.

Measurement:

- On the RMS-4 (Test setup), adjust switch [13] (EL 601) for an output level of +10 dBm.
- Connect the Z_x connector of the return loss measuring bridge directly to the P_I output [1] (Bu 1) of the unit being tested and read off the a_r value from the screen of the RME-4
  $a_r \geq 30$ dB (Error limit e)
- On the unit being tested, adjust the level step by step from 0 to -40 dBm with switch [13] (EL 601) and read off the return a_r from the screen at each setting $a_r \geq 34$ dB (Error limit e)

- Connect the Z_x connector of the measuring bridge directly to the P_{II} output [10] (Bu 502) and read off the a_r value from the screen.
  $a_r \geq 20$ dB (Error limit e)
- If the optional feature "IF calibration generator", BN 696/00.04, is fitted, then repeat the above measurements at the IF_o output [12] (Bu 1801)
  $a_r = 30$ dB (Error limit e)
- Change the equipment settings as follows:

  RMS-4 (Unit being tested): [13] (EL 601) : +10 dBm
  [9] (S 903) : 70 MHz

  RMS-4 (Test setup): [13] (EL 601) : -20 dBm
  [9] (S 903) : 140 MHz

  RME-4 (Test setup): [27] (S 1402) : 140 MHz

- Carry out calibration and measurement again as described above.

Connector	P_I [1]		P_{II} [10]	ZF_o [12]
Range [13]	+ 10 dBm	0, ..., - 40 dBm	-	-
a_r value	≧ 26 dB	≧ 30 dB	≧ 20 dB	26 dB

Table 8-3

8.4.2. Return loss of the BF connections

Required test equipment:

1 Level measuring set e.g. PSM-14 W&G
1 Return loss measuring bridge e.g. RFZ-5 W&G

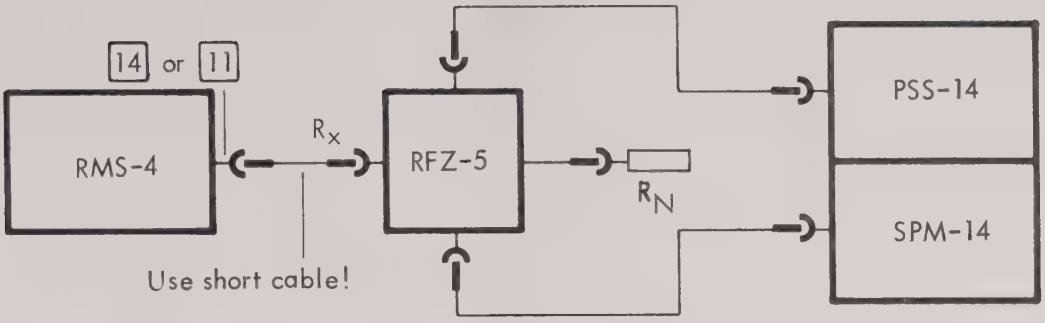


Figure 8-5 Test configuration for Section 8.4.2.

Equipment settings:

RMS-4: [8] (S 902) : Wideband
[15] (S 1601): Not depressed
[16] (P 1501): Fully anticlockwise
[17] (P 1305): Fully anticlockwise
[19] (S 1501): 0.093 MHz or 0.083 MHz

PSS-14: Output level approx. +8 dBm

SPM-14: Bandwidth 360 Hz, low-noise, f = 1 MHz

RFZ-5: Calibrated together with the PSM-14, R_N = 75 Ohm

- Connect the R_x connector of the return loss measuring bridge to output [14] (Bu 1605) of the RMS-4 (use a short cable!)
- Measure the return loss at the measuring frequencies (PSM-14 settings) with which the RMS-4 to be tested is equipped - see the f_M series on the scale of switch [19] (S 1501)
  $a_r \geq$ 30 dB (Error limit e)
- Repeat the measurement with one 20 dB pushbutton [15] (S 1601) depressed and with both 20 dB pushbuttons depressed
  $a_r \geq$ 30 dB (Error limit e)
- Now connect the R_x connector of the return loss measuring bridge to output [11] (Bu 1606) of the RMS-4
- Measure the return loss at the measuring frequencies 10, 80, 300 kHz, 1, 3, 10, and 13.6 MHz
  $a_r \geq$ 30 dB (Error limit e)

9. ADJUSTMENT INSTRUCTIONS

If the RMS-4 was repaired or if the check of technical data described in Chapter 8 detected values outside the specified error limits, then this chapter provides information on the necessary adjustments.

Unless otherwise specified, the adjustment should be carried out at room temperature (+23° C ± 3° C) and after a warming up period of 30 minutes.

Note: Wherever possible, the screening covers should remain in position on the printed circuits as the adjustment components are generally accessible through holes in the screening cases.

9.1. Adjustment of the supply voltage

Required test equipment:
1 Digital voltmeter e.g. 8000 A Fluke

The DC supply voltages are measured across capacitors C 1205, C 1215, and C 506 on the regulator boards [844-E] and [844-AC] of the power supply.

Adjustment is carried out as specified in Table 9-1

Supply voltage	Measured across	Adjust with
+12 V ± 0.5 %	C 1205	P 1201
-12 V ± 0.5 %	C 1215	P 1202
+ 5 V ± 0.5 %	C 506	P 501

Table 9-1 Adjustment of the supply voltages

9.2. Frequency adjustment

9.2.1. Adjustment of the IF center frequency

Required test equipment:
1 Digital frequency meter (up to 2 MHz) e.g. FZ-4 W&G

Equipment settings:

RMS-4: [34] (S 901) : U_A, U_M ext.
[4] (S 803) : Center frequency 70/140 MHz
[5] (P 802) : Center position
[9] (S 903) : 140 MHz

FZ-4: Measuring time 0.1 s

- Connect the digital frequency meter to socket [31] (Bu 802) on the rear of the RMS-4 (Output for 0.01 x IF)
- Adjust potentiometer P 801 on the discriminator board 696-W for a frequency indication of 1400 kHz $\pm$ 0.8 kHz

9.2.2. Adjustment of the measuring frequencies

Required test equipment:
1 Digital frequency meter (up to 20 MHz) e.g. FZ-4 W&G
1 Oscilloscope with 10:1 probe e.g. PM 3240 with Philips
probe PM 9350

Equipment settings:

RMS-4: [15] (S 1601) : not depressed
[16] (P 1501) : fully clockwise
[17] (P 1305) : fully anticlockwise

FZ-4: Operated with an external frequency standard with an accuracy of $\leq 1 \cdot 10^{-7}$
Measuring time: 1 s

Oscilloscope: Vertical sensitivity: 50 mV/Div.
Horizontal deflection: 50 ns/Div.

Adjustment of the lower measuring frequencies (< 1 MHz)

- The 3 low measuring frequencies are obtained from an oscillator whose frequency is measured and adjusted directly: connect the digital frequency meter to test point TP 1401 on the measuring frequency generation board [696-E...] or [696-AE] and adjust trimmers C 1422 for a frequency of (10)000.000 kHz $\pm$ 20 Hz

Adjustment of the high measuring frequencies (> 1 MHz)

- Connect the digital frequency meter to output [14] (BU 1605) and connect the probe of the oscilloscope to TP 1402 on board [696-E...] or [696-AE] ; adjust for maximum amplitude and correct frequency as specified in Table 9-2; the appropriate measuring frequency is selected with switch [19] (S 1501).

f_M frequency MHz	Amplitude adjustment with	Frequency adjustment with	Permissible deviation in Hz
(2) 400,000	C 1416	C 1435	± 5
(3) 580,000 [1)]	C 1414	C 1433	± 7
(3) 579,545 [1)]	C 1414	C 1433	± 7
(4) 430,000 [1)]	C 1414	C 1433	± 7
(4) 433,619 [1)]	C 1414	C 1433	± 7
(5) 600,000	C 1412	C 1431	± 11
(8) 200,000	C 1410	C 1429	± 16
(12) 390,000	C 1408	C 1427	± 25

Table 9-2 Adjustment of measuring frequencies > 1 MHz

9.2.3. Adjustment of the sweep frequencies

Required test equipment:
1 Digital frequency meter e.g. FZ-4 W&G

1) Optional feature

Equipment settings:

RMS-4: [4] (S 803) : Center frequency 70/140 MHz
[15] (S 1601) : Not depressed
[16] (P 1501) : Fully anticlockwise
[17] P 1305) : Fully clockwise

FZ-4: 10 µs periods

- Connect the digital frequency meter to output [14] (Bu 1605)
- Adjust the sweep frequencies on the sweep voltage oscillator board [696-H...] as specified in Table 9-3; the appropriate sweep frequency is selected with switch [20] (S 1302).

f_A frequency	Adjust with	Adjust to
70 Hz	P 1301	14.285 ms + 0.03 ms
18 Hz	P 1306	55.555 ms ± 0.11 ms

Table 9-3 Adjustment of the sweep frequencies

9.3. Level adjustment

9.3.1. Adjustment of the IF level P_I

Required test equipment:

1 Calibrated level meter with probe e.g. EPM-1 W&G

Equipment settings:

RMS-4: [2] (P 1201) : 0 dB
[13] (EL 601) : 0 dBm
[4] (S 803) : Center frequency 70/140 MHz
[9] (S 903) : 70 MHz
[34] (S 901) : U_A, U_M ext.

EPM-1: Measuring range ± 0.2 dBm
Calibrated with 0 dBm, R_i = 75 Ohm

- Connect the probe of the calibrated level meter socket [1] (Bu 1) of the RMS-4.

- Adjust potentiometer P 1203 on the reference generation and rectifier board [696-J] for an output level of 0 dBm ± 0.015 dB taking into account the frequency response error of the probe!)
- Change the level settings of the RMS-4: [2] (P 1201) to -10 dB and [13] (EL 601) to +10 dBm
- Adjust potentiometer P 1202 for an output level of 0 dBm ± 0.005 dB (taking into account the frequency response error of the probe!)

9.3.2. Adjustment of the measuring voltage U_M

Required test equipment:

1 Level measuring set e.g. PSM-7 W&G
1 Calibrated level meter with probe e.g. EPM-1 W&G

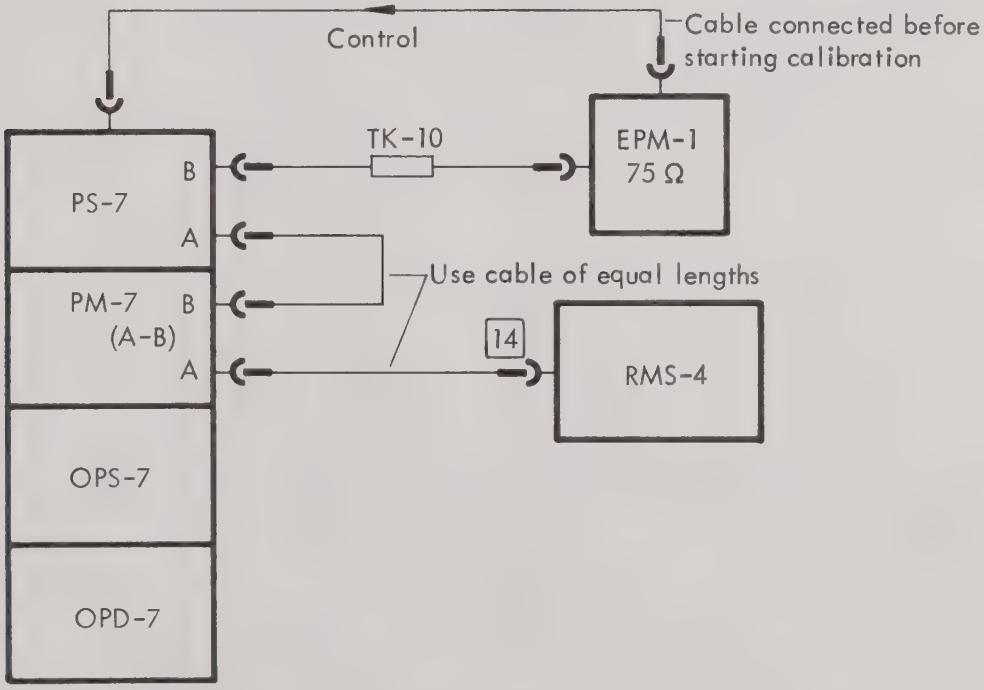


Figure 9-1 Test configuration for 9.3.2.

Equipment settings:

RMS-4: [4] (S 803) : CAL
[15] (S 1601): Not depressed

16 (P 1501): Fully clockwise

17 (P 1305): Fully anticlockwise

EPM-1: Measuring range ± 0.2 dBm
Calibrated with 0 dBm, R_i = 75 Ohm
Maximum control gain, control voltage 0 dBm

PS-7: Level setting 0 dBm

PM-7: Measuring mode A - B, bandwidth 2300 Hz, low distortion, fast display

- Set switch 19 (S 1501) on the RMS-4 to the measuring frequency 0.093 or 0.083 MHz.
- Adjust L 1509 on the U_M amplifier board 696-G or 696-AG for a maximum output level and then adjust P 1502 on the U_M control element board 696-U... for an output level of +5.23 dBm ± 0.04 dB
- At the following frequencies, shown in Table 9-4, first adjust the tuned circuit frequencies with L 15 ... or C 15 ... for a maximum level and then adjust P 15 ... for the correct output levels; before adjusting, set up the measuring frequencies f on the RMS-4 and the OPD-7

f/MHz	0.277 or 0.250	0.555 or 0.500	2.4	f_{sc} 1)	5.6	8.2	12.39
L or C	L 1508	L 1507	C 1530	C 1527	C 1524	C 1521	C 1519
Potentiometer	P 1509	P 1508	P 1507	P 1506	P 1505	P 1504	P 1503
Required value	+ 5.23 dBm					+ 5.18 dBm	
Adjustment tolerance	± 0.04 dB						

Table 9-4 Adjustment of the measuring voltage

1) f_{sc} Colour subcarrier frequency, option, if requested

9.3.3 Adjustment of the deflection voltage $\hat{U}_A$

Required test equipment:

1 Digital voltmeter	e.g. 8600 A	Fluke
2 DC power supplies	e.g. GS-2	W&G
1 Oscilloscope	e.g. PM 3240	Philips
1 $\hat{U}_A$ calibration device	constructed as shown in Figure 9-4 and Table 9-5	

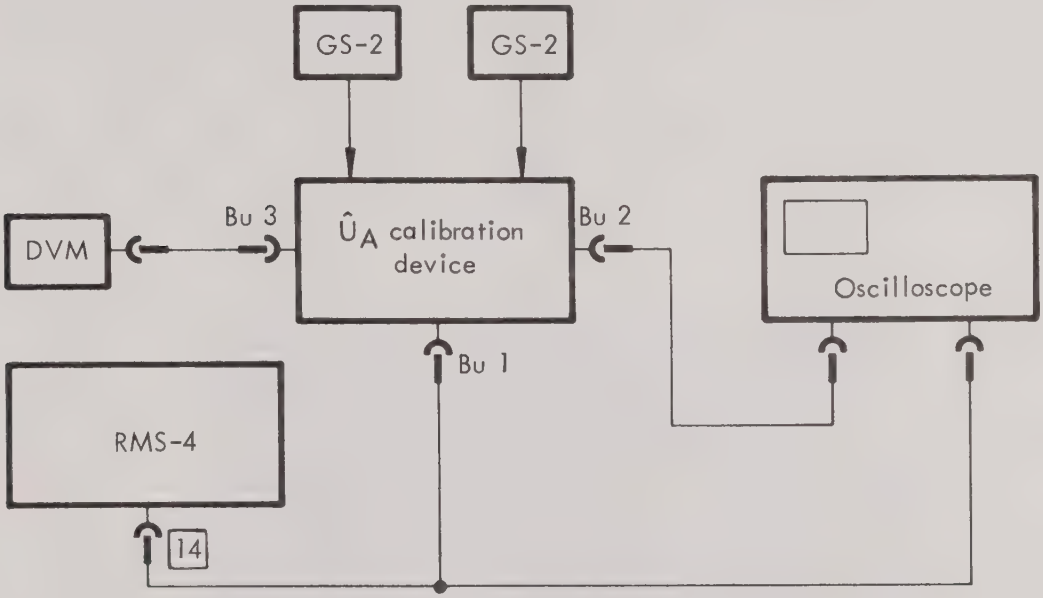


Figure 9-2 Test configuration for Section 9.3.3.

Equipment settings:

RMS-4:
[4] (S 803) : Center frequency 70/140 MHz
[7] (S 1301): OFF
[15] (S 1601): Not depressed
[16] (P 1501): 0 V (fully anticlockwise)
[17] (P 1305): 5 V (scale mark)
[20] (S 1302): 70 MHz

Oscilloscope: DC coupling, Y sensitivity, 50 mV/Div.
X sensitivity 2 V/Div.

Power supplies: $\pm$ 12 V $\pm$ 1 %

$\hat{U}_A$ calibration device: adjust potentiometer P 4 for a voltage of +5 V $\pm$ 5 mV (indicated on DVM)

- At f_A = 70 Hz, adjust potentiometer P 1307 on the explored range circuit board [696-AF...] or [696-AF...] for the oscillogram shown in Figure 9-3 and adjust for a spacing of $\pm$ 0.8 Div. (at 50 mV/Div). Adjustment is correct when both peaks are on a line.
- At f_A = 18 Hz, adjust the deflection voltage with potentiometer P 1302 for $\pm$ 0.8 Div.

A check of the accuracy is possible by varying the DC voltage with potentiometer P 4 of the $\hat{U}_A$ calibration device by 1 % = 2 Div. at 50 mV/Div.

Note: If the oscilloscope used cannot handle large signals, measuring errors may result.

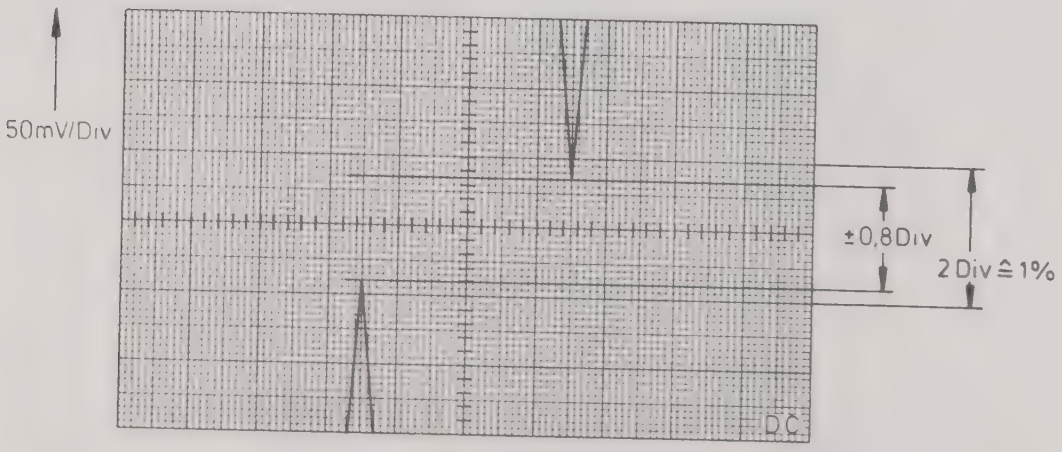


Figure 9-3

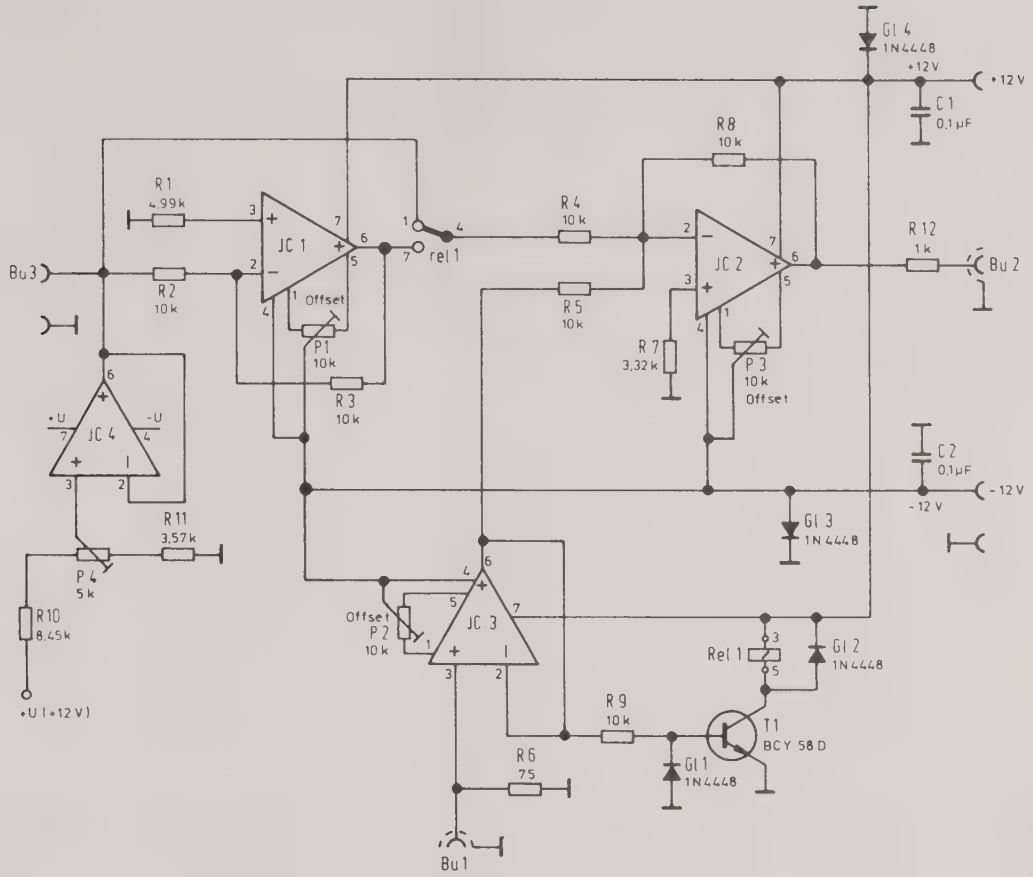


Figure 9-4 $\hat{U}_A$ calibration device

Part	Quant-ity	Designation	Electrical values	Ordering details	Name	Manuacturer,comments
R1	1	Composition resistor	4.99k/1%/Tk50/0207			WN 18/4/1
R2	1	"	10k/0.1%/Tk25/0207			"
R3	1	"	10k/0.1%/Tk25/0207			"
R4	1	"	10k/0.1%/Tk25/0207			"
R5	1	"	10k/0.1%/Tk25/0207			"
R6	1	"	75Ω/0.1%/Tk25/0207			"
R7	1	"	3.32k/1%/Tk50/0207			"
R8	1	"	10k/0.1%/Tk25/0207			"
R9	1	"	10k/1%/Tk50/0207			"
R10	1	"	8.45k/1%/Tk50/0207			"
R11	1	"	3.57k/1%/Tk50/0207			"
R12	1	"	1kΩ/5%/k12/0309			

Table 9-5 Parts list for $\hat{U}_A$ calibration device (Part 1 of 2)

Part	Quantity	Designation	Electrical values	Ordering details: Name	Manuacturer comments
C 1	1	Plastic foil capacitor	0.1 µF / ± 20% / 100 V		
C 2	1	"	0.1 µF / ± 20% / 100 V		
P 1	1	composition potentiometer	10k / lin / 0,5 W		1 WN 17/2/8
P 2	1	"	10k / lin / 0,5W		"
P 3	1	"	10k / lin / 0,5W		"
P 4	1	wire wound potentiometer	5 k Ω	071	WN 17/4/4 Contelec
Gl 1	1	Diode	1 N 4448		
Gl 2	1	"	"		
Gl 3	1	"	"		
Gl 4	1	"	"		
T 1	1	Transistor	BCY 59 D		
IC 1	1	IC	µA 741 C		
IC 2	1	"	"		
IC 3	1	"	"		
IC 4	1	"	"		
Rel 1	1	Relay	R HD - 12 V		WN 118/2/4 National, Japan SDS-Elektro

Ausgabe	Änderung	Tag	Name

	Tag	Name
Bearb		
Gepr		
Norm		

Wandel & Goltermann Reutlingen

Serie

Parts list

$\hat{U}_A$ calibration device

Liste ersetzt durch / Ersetzt für / Blatt Nr

Table 9-5 Parts list for $\hat{U}_A$ calibration device
(Part 2 of 2)

9.3.4. Adjustment of the explored range $\hat{\Delta F}_A$

Required test equipment and test configuration as in 9.3.3.
Before adjusting the explored range, check the sweep voltage as described in Section 8.2.3. and adjust it as described in Section 9.3.3. if necessary.

Equipment settings:

RMS-4:
- [4] (S 803) : Center frequency 70/140 MHz
- [6] (P 1303) : ± 30 MHz
- [7] (S 1301) : On
- [15] (S 1601) : Not depressed
- [16] (P 1501) : Fully anticlockwise
- [17] (P 1305) : 5 V (scale mark)
- [19] (S 1501) : 12.39 MHz
- [20] (S 1302) : 70 Hz

Oscilloscope and power supplies: as in Section 9.3.3.

$\hat{U}_A$ calibration device: Adjust potentiometer P 4 for a voltage calculated in accordance with the following formula:

$$U_{P4} = 5\ V\ (1 - \frac{f_M}{30}) \pm 0.1\ \%$$

f_M = highest measuring frequency installed in the RMS-4, specified in MHz

Example for f_M = 12.39 MHz

$$U_{P4} = 5\ V\ (1 - \frac{12.39}{30}) = 2.935\ V$$

- Adjust potentiometer P 1304 on the explored range circuit board [696-F...] or [696-AF...] so that the explored range voltage is as shown in the oscillogram in Figure 9-3 and adjusted for ± 0.4 Div (at 50 mV/Div.)

9.4. Adjustment of the effective deviation Δf

Required test equipment:

1 Receive section RME-4 of the radio link measuring setup RM-4 (W&G)

Equipment settings:

RMS-4:	[2]	(P 1201)	: 0 dB
	[13]	(EL 601)	: 0 dBm
	[4]	(S 803)	: Center frequency 70/140 MHz
	[8]	(S 902)	: Sweep
	[9]	(S 903)	: 140 MHz
	[17]	(P 1305)	: Fully anticlockwise
	[19]	(S 1501)	: 0.277 or 0.250 MHz
RME-4:	[29]	(S 1601)	: IF
	[31]	(EL 701)	: 0 dBm
	[36]	(S 1401)	: Tracking
	[37]	(S 1402)	: 140 MHz
	[15]	(S 1503)	: Bessel

- Connect output [1] (Bu 1) of the RMS-4 to input [27] (Bu 1) of the RME-4.
- Adjust potentiometer [16] (P 1501) for
  +4.74 dBm or 472.4 kHz at 0.277 MHz
  +3.82 dBm or 425.2 kHz at 0.250 MHz

A suitable setting mark is provided on the edge of the dBm scale, but this is visible only after removal of the coverplate. This mark is provided for measuring frequency 0.250 MHz only on series C units and later; for series B units, the setting must be interpolated or the level must be measured at socket (Bu 1605).

- Set up Bessel zero on the screen of the RME-4 with P 1601 on the U_M changover switch board [696-T] . Depress pushbutton [20] (S 901) on the RME-4 to improve the sensitivity.

9.5. Adjustment of the sweep width $\hat{\Delta F}$

Required test equipment:

1 Receive section RME-4 of the radio link test setup RM-4 (W&G)

Before adjusting the sweep width, the sweep voltage should be checked and, if necessary, adjusted as described in Section 9.3.3.

Equipment settings:

RMS-4:	[2]	(P 1201)	: 0 dB
	[13]	(EL 601)	: 0 dBm
	[7]	(S 1301)	: off
	[8]	(S 902)	: Sweep
	[9]	(S 903)	: 140 MHz
	[16]	(P 1501)	: Fully anticlockwise
	[17]	(P 1305)	: 25 MHz
	[18]	(S 801)	: 2 $\hat{\Delta}$F
	[20]	(S 1302)	: 70 Hz
	[34]	(S 901)	: Off (unmarked position)
RME-4:	[29]	(S 1601)	: IF
	[31]	(EL 701)	: 0 dBm
	[36]	(S 1401)	: Tracking
	[37]	(S 1402)	: 140 MHz
	[14]	(P 2203)	: Fully clockwise
	[9]	(S 2203)	: ΔP_I
	[11]	(S 601)	: 5 MHz

- Connect output [1] (Bu 1) of the RMS-4 to the input [27] (Bu 1) of the RME-4
- Calibrate the IF of the RMS-4; check that the frequency markers on the screen of the RME-4 are positioned symmetrically
- If the frequency markers are slightly asymmetrical, this can be compensated with the aid of the IF offset. The peak-to-peak sweep width remains unaffected by this:
  Set switch [4] (S 803) of the RMS-4 to the position "IF offset"; adjust potentiometer [3] (P 901) until the frequency markers are symmetrical.
- Adjust potentiometer P 803 on the discriminator board [696-W] so that the frequency markers are just visible at the start and end of the screen.

10 FUNCTIONAL DESCRIPTION

The Appendix with block diagrams and circuit diagrams of the assemblies should be used as an aid to understanding the following sections.

In the detailed assembly descriptions, the numbers in circles in the section headings refer to the number of the circuit diagrams in the Appendix.

10.1 FUNCTIONAL DESCRIPTION ON THE BASIS OF THE BLOCK DIAGRAM

10.1.1 IF SECTION

The heart of the IF generator is the HF oscillators. The intermediate frequency (45...190 MHz) is generated by mixing the carrier frequency (760 MHz) and the signal frequency (805...950 MHz).

The modulation oscillator (2) generates the carrier frequency which is modulated with the measuring frequency or, in the case of wideband operation, for noise distortion measurement, with the noise signal.

The sweep oscillator (10) generates the signal frequency. This, in contrast to the carrier frequency of the modulation oscillator, is modulated only with a low frequency voltage, which means that it can be called a sweep operation. The 1 GHz low-pass filter (11) suppresses the harmonics of the sweep oscillator in order to obtain a low distortion signal. The attenuators (3) in the mixer (3) improve the matching. The matching to the modulation oscillator is particularly important, as incorrect matching can affect the distortion results of the modulation oscillator.

The 460 MHz low pass filter (4) suppresses unwanted products from the mixer, and is used mainly to suppress the residual carrier signal.

The preamplifier (5) and final amplifier (6) amplify the IF level to a maximum of +10 dBm at output P_I of the unit. The variable attenuator [13] (E1 601) attenuates the IF level by a maximum of 50 dB in 10 dB steps.

In addition, the preamplifier provides an output for the frequency divider (8) and the IF output P_{II}.

10.1.1.1 Level control circuit

The final amplifier (6) is installed twice, the two amplifiers being connected in parallel. One branch leads to the output, the other to the measuring rectifier (12). Here, the IF level is compared with the reference volt-

age and the AGC amplifier (12) returns the control voltage to the control element (10) in the sweep oscillator.

The reference voltage is generated by limiting a 50 kHz TTL voltage and filtering out the basic frequency. The variation of the IF level is carried out with the aid of the control circuit by varying the reference with potentiometer [2] (P 1201). At the same time, a DC voltage which varies in synchronism with the variation of the reference voltage acts on the control element (5) in the preamplifier (5) and causes a maximum level change of 10 dB at this point. This achieves the following:

The IF level for the preamplifier remains basically constant, thus keeping the noise at the output of the unit also constant.

This is important in wideband mode, in order to ensure that the basic noise (measured in pWOp) does not exceed the required value over the whole range of the IF level.

The control element in the sweep oscillator must therefore only compensate for the overall frequency response and the non-linearity of the control element (5) in the preamplifier. The only frequency response which is externally noticeable is the difference between the frequency responses of the two parallel output amplifiers and the frequency response of the rectifier.

10.1.1.2 Frequency control circuit

The frequency control circuit has the tasks

- of keeping the center frequency constant
- of adjusting the sweep oscillator so that the generated frequency sweep is proportional to the applied sweep voltage,
- of permitting offset of the IF.

The frequency divider (8) is supplied with the IF from the preamplifier (5) and divides the frequency by a factor of 70 for IF = 35 MHz, by a factor of 140 for IF = 70 MHz, and by a factor of 280 for IF = 140 MHz.

This results in discriminator input frequency for IF_o of 500 kHz. The discriminator converts this frequency into a proportional voltage, which is compared with a DC voltage or with the sweep voltage in the AGC amplifier. The AGC amplifier adjusts the frequency of the sweep oscillator so that the difference at the input to the AGC amplifier becomes zero.

For calibration of the center frequency, the discriminator is fed with a crystal-controlled 500 kHz frequency and the output DC voltage of the dis-

criminator is adjusted until the two LEDs of the comparator circuit are both off. The IF now lies within the required tolerance.

The frequency control receives a sweep voltage with a maximum amplitude of 10 V_{pp} and generates from this voltage a frequency sweep of $\pm$ 50 MHz for IF = 140 MHz if switch [8] (S 801/11) is set to 2 Δ^{A}F. If this switch is moved to the other position, the sweep voltage is divided by a factor of 2, and the frequency sweep is thus only 25 MHz. In the 70 MHz range, this switch has no effect; nevertheless, a sweep of only 25 MHz is generated because the steepness (MHz/V) is reduced by a factor of 2 due to the reduced frequency division factor.

In the 35 MHz range, switch [8] (S 801/11) is likewise non-functional. Because of the small division of frequency the steepness (MHz/V) is a factor of 4 smaller than at 140 MHz and in addition the sweep voltage is divided by a factor of 2.5 so that the 5 MHz sweep width remains.

The IF offset is achieved by adding a DC voltage to the sweep voltage; the offset is $\pm$ 12.5, $\pm$ 25 or $\pm$ 50 MHz including the sweep width. In the 140 MHz range, for example, with a sweep width of $\pm$ 10 MHz, a maximum offset of + or -40 MHz is possible.

This offset is easily checked with the aid of the divider output [31] (Bu 802, 100:1) and a counter.

10.1.1.3 Wideband operation

In the wideband mode, the BF input [11] (Bu 1606) is connected to the modulation oscillator. The lower limit frequency of the frequency control circuit is now sufficiently low (approx. 0.1 Hz) to permit transmission of a square-wave signal with a frequency of 50 Hz and a ramp-off value of less than 1 %. (This signal form is found in TV transmissions). The frequency control circuit now only controls the constancy of the center frequency.

The internal connections - U_M voltage to the modulation oscillator and the U_A voltage to the sweep oscillator - are thus disconnected in this mode (rel 1603, rel 1602, [8] (S 902/1)).

10.1.1.4 Headset operation

If the headset is switched from "Measure" to "Speech" the input of the modulation oscillator is connected to the headset socket ([33] (Bu 1603/4), rel 1604), and the control circuit is simultaneously switched to wideband mode.

10.1.1.5 U_A, U_M ext. operation

This operating mode is provided to permit operation with an external distortion measuring set (e.g. VZM-3). The changeover switch [34] (S 901) is located on the rear of the unit, as is the input for the external sweep voltage U_A [35] (Bu 901). A red LED indicates that U_A, U_M ext. mode has been selected.

The BF input [11] (Bu 1606) is now the input for the external measuring voltage U_M. The switch "Sweep-wideband" [8] (S 902) now only has the function "Sweep" even if it is set to the position "Wideband".

The inputs U_A, U_M ext. have a steepness of 10 MHz/V.

10.1.2 BF SECTION

10.1.2.1 U_M path

The measuring frequencies are generated by division of the signal from a 10 MHz quartz oscillator and an oscillator with 5 separately switchable quartz crystals (14). The last element in the divider chain is a 2:1 divider which provides a precise duty cycle of 1:1. This is important because the basic frequency is filtered out of the square-wave signal in the U_M amplifier (15) and the height of the basic frequency voltage is also a function of the duty cycle.

In the limiter (15), the TTL voltage, whose amplitude is uncertain, is converted to a defined amplitude which is proportional to the angle of rotation of potentiometer [16] (P 1501). This potentiometer is thus used to set up the measuring voltage U_M.

Via a 15 MHz low-pass filter and an amplifier the U_M voltage is fed through one path, a 20 dB attenuator, to the modulation oscillator (2) and through a second path, a 20 dB attenuation switch to the output splitter (16).

The 500 kHz calibration frequency (calibration of the IF center frequency, triggering of the IF calibration generator (8)) and the reference frequency (for the rectifier) are also derived from the 10 MHz oscillator.

10.1.2.2 U_A path

The U_A voltage generated in the deflection voltage oscillator (13) is connected via an isolating amplifier, a summing amplifier, and the U_A final amplifier (16) to the output switch.

The frequency of the deflection voltage can be switched between 18 and 70 Hz with switch [20] (S 1302).

The explored range circuit (13) is a device which varies the sweep voltage when the measuring frequency is switched such that an explored range set up with potentiometer [6] (P 1303) is not exceeded.

A further circuit observes the frequency and signals when the current measuring frequency is greater than the explored range.

A gap for detection, with correct phase, of the distortion results in the receive section RME-4 in the mode "BF receive" can be inserted with switch [21] (S 1303). The gap is injected into the measured voltage at a time corresponding to the negative peak value of the sweep voltage.

10.1.2.3 Output switch

The signals U_A and U_M are combined to form the test signal $U_A + U_M$ in the output switch.

The high-pass and low-pass filters are necessary in order to prevent generation of distortion by the internal amplifiers. The output signal $U_A + U_M$ can be attenuated by 20 dB before it is connected to the socket [14] (Bu 1605).

10.1.3 ADDITIONAL FEATURES (OPTIONAL)

10.1.3.1 IF calibration generator 70 and 140 MHz (quiet tone)

This is a phase-controlled oscillator with the 500 kHz calibration frequency as the reference frequency. The frequency can be switched with switch [9] (S 903).

Due to its phase regulation, the oscillator has crystal accuracy ($\pm 2 \cdot 10^{-5}$) and has a very low sideband noise value.

10.1.3.2 Color subcarrier oscillator

This oscillator is installed in the measuring frequency generation circuit (14) and can generate the frequencies 3.579545, 4.433619, 3.58, or 4.43 MHz. The oscillator operates at twice the selected frequency as the frequency is subsequently divided by a factor of 2 in the measuring frequency generation circuit (14).

The oscillator is switched on with the measuring frequency selection switch [19] (S 1501).

10.1.3.3 IF offset with high resolution

In this case, the normal potentiometer [3] (P 901) is replaced by a 10-turn helical potentiometer with a counter device, which permits a resolution of 25 or 50 kHz and simultaneously permits setting of the IF frequency with an accuracy of 250 or 500 kHz without the necessity of a frequency counter.

10.2 DETAILED ASSEMBLY DESCRIPTIONS

10.2.1 POWER SUPPLY (1)

The power supply consists of the main groups mains input with mains filter, fuse and voltage selector, mains transformer, rectifier, filtering and regulation.

The secondary voltages generated in the mains transformer are rectified, filtered, and passed on to the regulators or stabilization circuits.

The reference voltages for the stabilized voltages are obtained by means of voltage dividers from the + and -12 V standard voltages (+12 V standard regulator).

The +12 V supply has no auxiliary voltage. The -12 V supply obtains its auxiliary voltage by means of half-wave rectification, which is derived from the main voltage. The 5 V supply uses the auxiliary voltage of the +12 V output.

The supply voltage for a stabilized +16 V supply is taken from the excess voltage of the +12 V regulator. The reference voltage for stabilization is obtained from the regulated output voltage of the +12 V regulator.

A -21 V supply (stabilized) obtains its input voltage from a -33 V supply, which is obtained by addition of the regulated -12 V and an unregulated -21 V supply. The corresponding reference voltage is taken from the regulated output of the -12 V regulator.

A -16 V supply (stabilized) receives the excess voltage from the stabilized -21 V supply and its reference voltage comes from the regulated -12 V output. Stabilization of the -21 V, -16 V, and +16 V supplies is carried out in the assembly frequency control (9), which is physically separate from the power supply.

10.2.2 SWEEP OSCILLATOR (10) AND MODULATION OSCILLATOR (2)

The sweep oscillator (signal oscillator; f = 830 MHz ± 25 MHz or 900 MHz ± 50 MHz) is controlled by a frequency control circuit such that the difference between its frequency and that of the modulation oscillator (carrier oscillator; f = 760 MHz) at the output of the mixer results in an IF of 70 MHz ± 25 MHz or 140 MHz ± 50 MHz, according to the equipment settings.

In both oscillators, the resonant circuit is a common base stage with feedback. The collector is connected to the DC zero potential.
The -12 V supply is connected via a coaxial λ/4 line with a capactive short circuit in series with a ferrite choke to the emitter resistor.

This circuit provides decoupling and prevents gaps and peaks in the tuning range. The same applies to the λ/4 line between the tuned circuit and the input for the sweep or measuring voltage.

The feedback voltage is taken from a tap on the collector inductance L 1004 or L 204 via trimmer C 1005 or C 208 (tuning) to the emitter. The output - a tap slightly higher on the inductance - provides +10 dBm into 50 Ω.

10.2.2.1 Sweep oscillator (10)

The sweep range 805 MHz...950 MHz can be adjusted with C 1004; the sweep voltage is inserted at pin (10) 38. The HF output voltage is connected via a PIN diode control element to pin (10) 41.

An attenuator with a value of 4.2 dB is connected between the oscillator and the PIN diode control element in order to improve the load return loss.

10.2.2.2 Modulation oscillator (2)

Here, modulation with the measuring voltage (pin (2) 46) is carried out. The requirement for low steepness distortion (small deviation from the linear relationship between frequency and measuring voltage) requires that the relationship $C_{loop} = \frac{1}{U_M^2}\ k$ be maintained as accurately as possible.

The tuned circuit is dimensioned such that the above relationship can be approximated by an inductance parallel to the capacitance diode G1 202 for a favorable working point on the characteristic of the capacitance diodes ($U_R \approx 9$ V$\rightsquigarrow f_{Tr}$ = 760 MHz, adjustable with potentiometer P 201.

It is implemented by the λ/4 line, for which trimmer C 205 provides a capacitive load. The inductance is adjustable in order to permit compensation for the tolerances of the capacitance diodes Gl 201, Gl 202, and the capacitances of transistor T 201.

C 206 and R 207 have the task of tuning the line resulting between the external conductor of this λ/4 line and the circuit board ground and damping it so that its effect on the tuned circuit remains low.

The choke L 202 and the following λ/4 line, which is capacitively short-circuited for HF with C 207 and C 210, is used for further decoupling of the tuned circuit.

As, due the required modulation response up to 14 MHz, C 207[1]) cannot be made sufficiently large to keep C 210 sufficiently free of HF, the connection wires of C 201 are fitted with ferrite rings. These reduce the effect of the ground capacitance of C 201 on the distortion alignment.

R 208 was connected in series in order to damp the resonance of C 201 with L 205, L 206 (approx. 200 kHz).

10.2.3 1 GHZ LOW-PASS FILTER (11)

The 1 GHz low-pass filter is a 9th order filter constructed in printed conductor technology. It is intended to improve the harmonic ratio of the signal from the sweep oscillator to 40 dB or greater.

10.2.4 MIXER (3)

The signal frequency 830 MHz ± 25 MHz or 900 MHz ± 50 MHz is converted to 70 MHZ ± 25 MHz or 140 MHz ± 50 MHz, respectively, in the ring modulator IC 301. The carrier input to this modulator is supplied with 760 MHz (+10 dBm) by the modulation oscillator.

Attenuators with a value of 5.4 dB are connected between the signal and carrier inputs and the ring modulator in order to reduce the distortion due to incorrect matching. A high return loss at the carrier input of the mixer is particularly important as this has a large effect on the distortion of the modulation oscillator.

Adjustment is carried out with C 305, the adjustment criteria being distorted in the wideband path.

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1) Not fitted in Series C units and later

10.2.5 460 MHZ LOW-PASS FILTER (4)

The low-pass filter is a printed conductor filter of the 9th order and is used to suppress residual carrier and signal frequencies.

In order to present an impedance of approximately 50 Ω to the mixer, even at high frequencies, a resistor is fitted in series with the first capacitor. The advantage of this is an increased attenuation of the unwanted mixer products.

10.2.6 PREAMPLIFIER (5)

In addition to the actual preamplifier in which the transmitted signal is amplified aand passed on to the final amplifier, the preamplifier contains the following functional groups:

- the control element for 10 dB level variation,
- the fequency divider output;
- The P_{II} output [10] (Bu 502)

The actual amplifier IC 501 is a thick film amplifier with V = 12 dB. The following common emitter stage provides the remaining gain of 6.5 dB. The frequency response can be adjusted with C 523. The signal is extracted at the collector of transistor T 501 and connected via the control stage T 503 to the output amplifier (6).

The level variation is achieved with a variable negative feedback in the emitter; the variable resistor is the PIN diode G1 501. The network L 504, P 502 compensates for the capacitance at the emitter, which has a greater effect as the resistance of the PIN diode increases. The harmonic distortion at low levels is adjusted with potentiometer P 502.

The networks R 515, C 512 and R 531, C 524 compensate for the lower corner frequency of IC 501 and prevent distortion in the 70 MHz area.

The controlling voltage for the PIN diode G1 501 is fed from pin (5) 57 of the impedance transformer IC 502/4.1. In order to prevent amplitude modulation of the IF by the 50 kHz reference frequency that is present on point (5) 57, the inverting amplifier IC 502/4.2 has a cut-off frequency of 1.6 Hz. From the control voltage the transistor T 502' and resistor R 518 derive a control current for the PIN diode G1 501; T 502 at the reference input of IC 502/4.3 compensates for the temperature caused drift of T 502'. The gain of the preamplifier is adjusted by P 501, which adjusts the current through the PIN diode G1 501 so that the current is set at 0 dBm. P 503 ad-

justs the gain at -10 dBm. IC 502/4.4 acts as a voltage source for the compensation circuit with T 502.

A further common emitter stage extracts the signal from the collector of transistor T 501; this supplies the frequency divider (8). The voltage for the P_{II} output stage is extracted from the collector of transistor T 504.

The input impedance of the stage with T 505 is 75 Ω, and the level at this point is adjusted to -6 dBm with potentiometer P 504 (applies to Series C units and later).

The frequency response of this output is the frequency response of the output amplifier, of the control stage T 503, and of the emitter stages T 504, T 505. The reason for this is that the level is controlled only after the final amplifier.

10.2.7 FINAL AMPLIFIER (6)

The amplifying stage is transistor T 603 with voltage negative feedback (R 616) and current negative feedback (R 617, R 622). The gain is 10 dB and the output level is +10 dBm into 75 Ω. The return loss is adjusted with trimmers C 628 and C 630. A good frequency response of the amplifier stage is achieved if it is supplied from an impedance of 50 Ω. This is carried out by transistor stage T 601 with unity gain.

The amplifier stage T 603 has an "electronic" internal impedance, i.e. it presents an impedance of Z = 75 Ω but the point with $R_i = 0$ is not accessible. As this means that it is not possible to provide the second output for the rectifier with low decoupling, the final amplifier is installed twice. This has the additional advantage that the requirements for the frequency response of the amplifier do not need to be so extremely high as would be the case if the branch to the rectifier would exist before the final amplifier. With the configuration used here, only the difference in the frequency responses and the difference in the temperature coefficients affect the frequency response and the level accuracy.

The chip components are necessary in this amplifier due to their low inductance values.

The inductance L 610 is used for compensation of the return loss at the input and the networks R 626, R 628, L 608, C 630, and R 627, R 629, L 609, C 631, provide the output return loss.

The frequency response of the amplifier stages is adjusted by trimmers C 605 and C 636.

The output signal is connected to the front panel of the unit via the variable attenuator [13] (EL 601). This attenuator has a total attenuation of 50 dB, which can be switched in 10 dB steps. The attenuator elements in the variable attenuator are implemented in thin film technology.

10.2.8 FREQUENCY CONTROL CIRCUIT

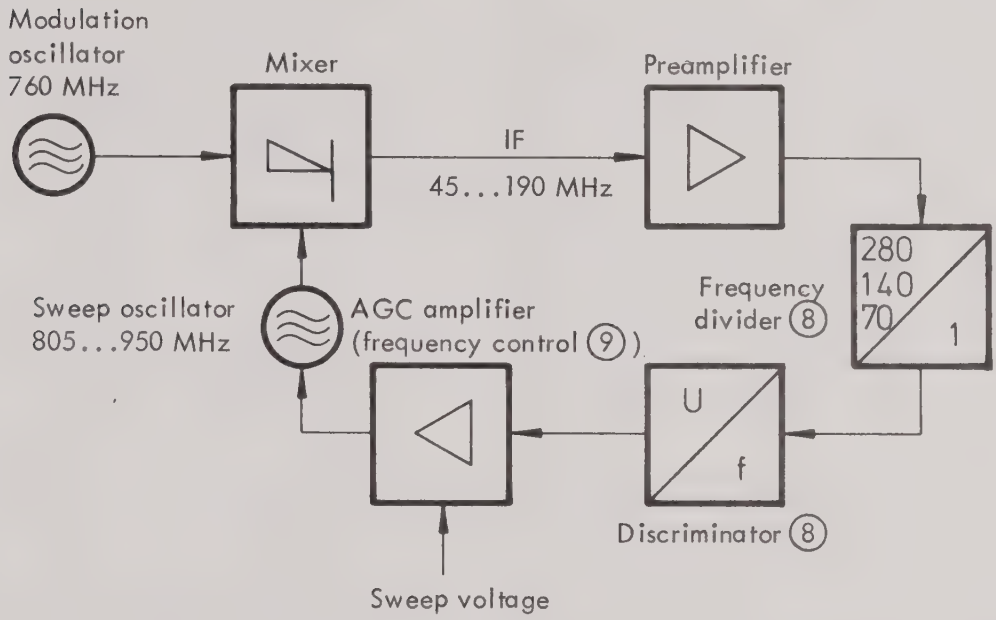

Figure 10-1 Basic circuit of the frequency control circuit

The IF is generated by mixing the two oscillator frequencies. The IF signal is amplified by the preamplifier and connected to the frequency divider, which divides the frequency such that a constant discriminator input frequency of 500 kHz results for IF_0 = 35, 70 or 140 MHz. The discriminator converts this frequency into a proportional voltage, which is compared with a DC voltage or with the sweep voltage in the AGC amplifier. This amplifier then adjusts the frequency of the sweep oscillator until the difference at the input of the AGC amplifier becomes zero.

The assemblie's frequency divider and discriminator (8) and frequency control (9) are described in more detail in the following sections.

10.2.8.1 Frequency divider (8)

The input stage consists of a common base stage T 801 with a following common collector stage T 802. This common collector stage limits the signal such that there are no spikes below 0 V and above +5 V, as less then 0 V and greater +5 V are impermissible ranges for the following 10:1 ECL divider IC 801 (ECL = emitter coupled logic). The input level is > 0 dBm and the limits of its sensitivity are shown in Figure 10-2.

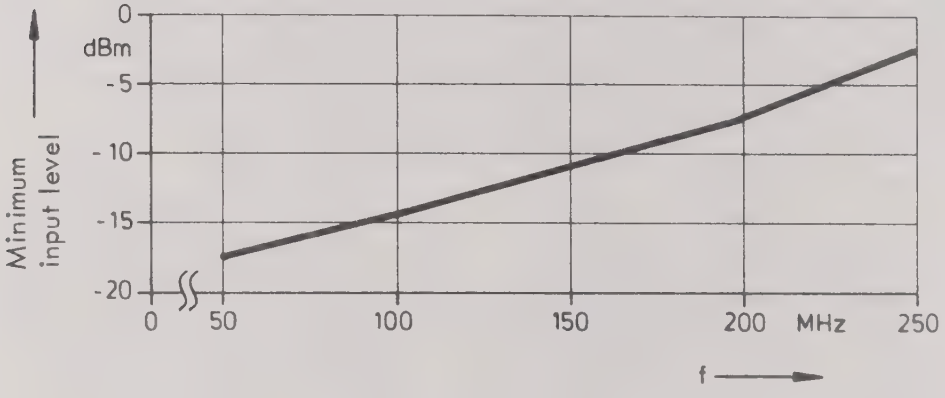

Figure 10-2 Minimum input level of the frequency divider

Transistor T 803 converts the ECL level into a TTL level; this is followed by a 2:1 divider (IC 803/2.1) that is switched to 1:1 at 35 MHz IF, and a 7:1 divider (IC 804).

A further 2:1 divider (IC 803/2.2) is switched to 1:1 when an IF of 35 or 70 MHz is selected, so that the output of the frequency divider is a 500 kHz signal when the IF is 35, 70 or 140 MHz.

In the case of calibration, IC 805/4.2/4.4 connects the 500 kHz calibration frequency coming from the divider chain in the BF section to the discriminator. Together with IC 801 and IC 803/2.1, the 5:1 divider IC 802 forms a 100:1 frequency divider at whose output the IF can be checked with a digital frequency meter. (Divider output [31] (Bu 802) on the rear of the unit.

10.2.8.2 Discriminator (8)

The discriminator is designed as a counting discriminator. The pulses are generated by the monoflop IC 805 and their amplitude is controlled by the limiter IC 807/4.2/4.3.

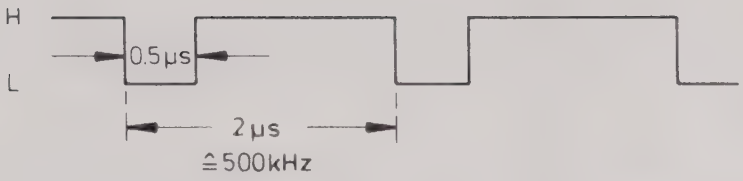

Figure 10-3 High and low phases of the monoflop IC 806

During the high phase, transistor IC 807/4.3 is cut off and a current I flows into capacitors C 828 and C 834. In the low phase, the transistor conducts, sinking the current I from the current source T 805 and additionally drawing a current of 3 I from capacitors C 828 and C 834. However, as the low phase is only 1/4 of the cycle, the charge on the capacitor - averaged over one cycle is equal to zero.

If precisely 500 kHz is connected to the input of the discriminator, the voltage at pin 3 of IC 808/2.2 can be adjusted precisely to zero with the potentiometers P 901 and P 802. This is the calibration case! Potentiometer P 801 and R 826 compensate for the basic tolerances in the monoflop and in the discriminator, and the drift and the temperature coefficient are equalized with the potentiometer (P 802).

The steepness of the discriminator is adjusted with potentiometer P 803, this being 8 V/50 MHz at 140 MHz, 8 V/25 MHz at 70 MHz, and 8 V/12.5 MHz at 35 MHz at pin 1 of IC 802/2.2.

The pulse length of monoflop IC 806 was made so small so that the highest IC (190 MHz) can still be processed in the 70 MHz range.

With a duty cycle of 1:1 (pulse length 1 µs), the trailing edge of the pulse would fall within the active time of the monoflop and would be ignored. However, this would mean an incorrect voltage at the output of the discriminaator, and the regulator could not adjust the frequency from 190 MHz to 95 MHz, as is required.

10.2.8.3 Frequency control

The actual value is compared with the required value in IC 904. The required value cana be either 0 V (in the position "Center frequency" of switch [4] (S 803)) or a variable DC voltage (in position "IF offset" of switch [4] (S 803)). The deflection voltage can also be added to these voltages. The internal deflection voltage is connected to pin (9) L.

It can be reduced by a factor of 2 at 140 MHz through the switching of divider R 908, R 912, R 909, and by a factor of 2.5 at 35 MHz through divider R 908, R 907, R 909.

The deflection voltage is connected to the reference input of the AGC amplifier via the isolating amplifier IC 902/4.1 and the summing amplifier IC 902/4.4.

Switch [34] (S 901/1) provides switching between the internal and external deflection voltage inputs. The modulation steepness at socket [35] (Bu 901) is 10 MHz/V.

Because of the modulation steepness being independent from the selected IF, the discriminator steepness alters with the IF changeover, so the gain of IC 901 must be accordingly switched. Compared to the 140 MHz IF the gain at 70 MHz IF is reduced by a factor of 2 and the 35 MHz IF is reduced by a factor of 4.

IC 902/4.2-4.3 generate the voltage for the IF offset, which is adjusted with potentiometer [3] (P 901). If the RMS-4 is equipped with a 10 turn helical potentiometer with counter instead of potentiometer [3] (P 901) (optional feature!), then the upper and lower frequency limits are set with potentiometers P 904 and P 905.

The AGC amplifier IC 904 acts as P_I controller in sweep mode; an additional time constant (R 933, C 917) provides a 20 dB/decade drop at high frequencies. The DC voltage offset of approximately -10 V necessary for the center working point of the sweep oscillator is generated with IC 905 and the current source T 904. In this case, the AGC amplifier operates at approximately 0 V and switching of the loop gain with R 938, R 940, P 903 and switch T 907 is carried out without an additional DC voltage offset. This loop gain switching is necessary because the loop gain is changed when the frequency divider is switched by a factor of 2 (280 ⟶ 140).

In wideband mode, the AGC amplifier is converted to an I controller. In this case, only the modulation oscillator is driven and the sweep oscillator is not permitted to compensate for these signals.

In particular, the generator must be capable of transmitting 50 Hz square-wave signals with a ramp-off of 0.5 %. For this reason, it is necessary to make the lower limit frequency of the control circuit very low. The time constant is switched with the aid of transistor T 902 and relay Rel 901. With the components installed in the unit, the ramp-off is approximately 4 %. Compensation of the ramp-off to the required value is carried out by the modulation oscillator (2). In instruments from series C onwards, the use of a different operational amplifier (IC 904) and an increase in the value of resistor R 919 and R 920 makes compensation unnecessary.

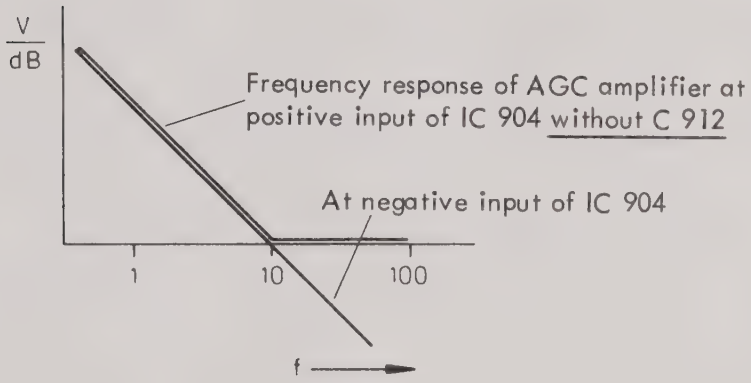

Figure 10-4 Frequency response of the AGC amplifier

Figure 10-4 shows the frequency response of the AGC amplifier at the positive input without C 912.

With a square-wave input voltage, this frequency response results in the waveforms shown in Figure 10-5. As square-wave input signals occur during the setting operation with IF center frequency offset, this unwanted behavior is corrected. This is done by connecting C 912 to the positive input of IC 904, thus making the frequency response at the positive and negative inputs of the AGC amplifier identical.

In the case of calibration (switch [4] (S 803) in position "CAL"), the circuit checks whether the voltage at point d is zero, pin (9) K being connected to ground with switch [4] (S 803/C). The circuit is also switched to sweep mode and the AGC amplifier is converted to a linear amplifier. Transistor T 903 connects R 934 parallel to the PI network, which means that the amplifier has a gain of V = 280.

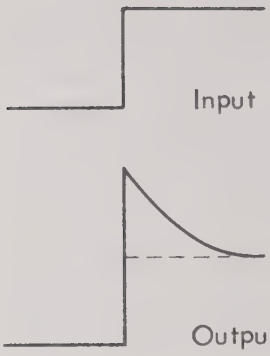

Figure 10-5 Waveform at the output of the AGC amplifier in the case of a square-wave input signal

A voltage difference of 16 mV at the input of the amplifier indicates a frequency deviation of 100 kHz at IF = 140 MHz or 50 kHz at IF = 70 MHz. With a voltage difference of 11.86 mV x 280 = 3.32 V, the comparator IC 906. IC 907 reacts and signals either "Frequency too high" or "Frequency too low". 11.86 V means a frequency deviation of 74 kHz or 74 kHz.

The difference from the guaranteed value of 100/50 kHz is required mainly for wideband operation, because the control fluctuation is greater due to the larger resistors (R 913, R 920) and because calibration is carried out in sweep mode.

10.2.9 REFERENCE GENERATION AND RECTIFIER (12)

10.2.9.1 Reference generation

The reference frequency is obtained in the measuring frequency generation circuit (14) by dividing the 10 MHz quartz frequency and is 50 kHz. The TTL level is adjusted to a defined amplitude in the limiter IC 1201. The low-pass filter C 1203, C 1204, L 1201 filters the basic frequency out of the 50 kHz square-wave signal, which means that a sinusoidal voltage with a defined amplitude and good stability is available at IC 1201/5.5, pin 7. The temperature coefficient and the amplitude of this voltage depend practically only on the following components: Gl 1201, R 1205, R 1204, and R 1209.

The reference level can be reduced by 10 dB with potentiometer [2] (P 1201), resulting in a similar reduction in the output level via the level

control loop. Parallel connection of resistor R 1213 between the lower end of the potentiometer and the wiper of the potentiometer provides a linear dB scale on the knob of potentiometer.

The -10 dB point is adjusted with P 1202. IC 1202 extracts the voltage from the potentiometer with high impedance and amplifies it to the necessary reference level. Transistor T 1201 in the negative feedback path provides the necessary power. The absolute level of 0 dBm is adjusted with potentiometer P 1203.

10.2.9.2 Rectifier

The rectifier consists of a measuring path and a reference path. It is constructed as a pseudo-RMS voltage-doubler rectifier. The bias currents through the rectifier diodes are adjusted with potentiometers P 1204, P 1205, and P 1206.

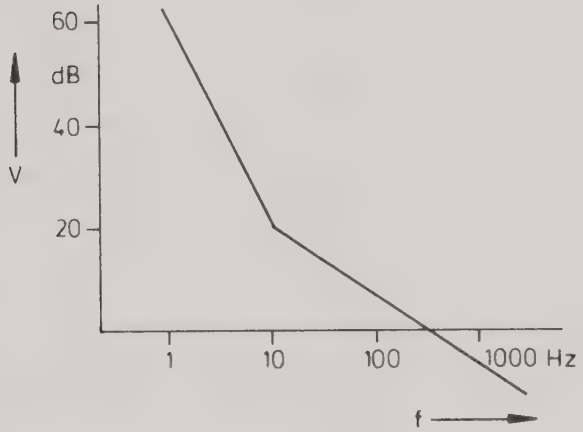

Figure 10-6 Gain characteristic of the AGC amplifier IC 1203

The voltage difference between the two rectifiers is observed by an AGC amplifier, which acts on the control element in the sweep oscillator such that the difference becomes zero, which means that the HF level at the measuring rectifier is equal to the reference level.

The AGC amplifier IC 1203 is constructed as an I controller, in which the gain increases at a rate of 40 dB/decade at frequencies below a specific value.

The network following the AGC amplifier is necessary for control stability and to reduce the loop gain. Transistor T 1202 decouples this network from the control element input. The loop gain is adjusted with potentiometer P 1208, the input offset voltage being adjusted with P 1207.

10.2.10 DEFLECTION VOLTAGE GENERATION (13)

10.2.10.1 Deflection voltage oscillator

The deflection voltage is generated by a Wien-Robinson oscillator that has stabilized output voltage. The frequency determining components are C 1315, C 1316, R 1361...R 1366, P 1301 and P 1306 and are placed in the coupling branch of the IC 1306 amplifier. The controlling element for the output voltage stabilization is a field effect transistor T 1317 acting as a controllable resistor in the feedback path. The output voltage from the oscillator is fed to the input of differential amplifier T 1315/T 1316 via amplifier IC 1307 and R 1375. At the other input of the differential amplifier a reference voltage of -5.1 V is applied by Zener diode G1 1319. The negative half-wave of the oscillator output voltage is compared to the reference voltage and T 1317 is so controlled through T 1315 that the oscillator output voltage has a certain constant quantity. During the positive half-wave, C 1317 stores the control voltage for T 1317. The time constant C 1317 and T 1317 is larger than the period of the lowest deflection frequency.

Potentiometers P 1301 and P 1306 are used for adjusting the deflection frequencies, 70 Hz and 18 Hz. If requested by the customer, the frequency determining components can be changed so that frequencies can be produced in the range for 18 Hz to 100 Hz.

The deflection voltage phase position is shifted by 90° through differential amplifier IC 1308/2.1.

Now when the push button "GAP" is depressed, the comparator IC 1308/2.2 switches at the zero crossings, that is, at the positive and negative deflection voltage peaks. The negative transitions are differentiated in the U_M controlling element (15) and are momentarily reduced.

10.2.10.2 Explored range circuit

The explored range is half of the bandwidth which is necessary to permit transmission of a specific sweep width $\Delta^{\bullet}F$ and a specific measuring frequen-

cy f_M with frequency modulation (a prerequisite is that practically only the first sidelines of the measuring frequency exist).

For transmission of f_M = 12.39 MHz and $\hat{\Delta}F$ = 10 MHz,,for example, a half bandwidth of 22.39 MHz is necessary.

However, as the bandwidth available is constant - determined by the equipment being tested - but the measuring frequency is varied in the method used in the RM-4 for measurement of distortion, the only solution is to reduce the deviation if the bandwidth is not to be exceeded by the test signal at high measuring frequencies. In order to fulfill this requirement, the explored range circuit must fulfill the following function:

$$U_A = A \cdot (1 - \frac{f_M}{\hat{\Delta}F_A}) \cdot U_{A_o} \cdot B$$

U_{A_o} is the voltage provided by the deflection voltage oscillator, which is available at IC 1302/4.1, pin 8.

A is the factor with which the voltage U_A can be reduced with potentiometer [17] (P 1305).

f_M is the measuring frequency, adjustable with dividers controlled by the measuring frequency switch [19] (S 1501)

$\hat{\Delta}F_A$ is the explored range

U_A is the voltage which is available at output [14] (Bu 1605) or causes the sweep width $\hat{\Delta}F$.

B is the general amplification factor.

The deflection voltage is amplified by IC 1302/4.1. After that inverting amplifier IC 1302/4.2 supplies a gain of $V = \frac{R\ 1307 + P\ 1304}{P\ 1303}$. The output voltage is now divided by R 1312 and each resistor, according to the switched-in measuring frequency, R 1322, R 1325, R 1330, R 1333, R 1337, R 1341, or R 1356. Amplifier IC 1303/2.1 offers a high input impedance for the divided deflection voltage. Because of P 1303 now being proportional to the explored range $\hat{\Delta}F_A$, and the division after IC 1302/4.1 is proportional to the measuring frequency f_m, the term $-U_{A_o} \frac{f_m}{\hat{\Delta}F_A}$ of the above function is fulfilled. The adding amplifier IC 1303/2.2 now forms the difference $U_{A_o} - U_{A_o} \frac{f_m}{\hat{\Delta}F_A}$. Potentiometer P 1305 permits decreasing the difference voltage.

If the controls are set incorrectly, it is possible to select a greater measuring frequency than the selected explored range. If this case occurs, the gain between IC 1302/4.1, pin 8, and IC 1303/2.1, pin 7 becomes greater than 1, but the permissible value is less than or equals 1. The rectifiers Gl 1305 and Gl 1311 and the comparator IC 1302/4.4 check for this condition.
If the gain V = 1 is exceeded, relay contact rel 1601 opens, causing the sweep width to become zero. At the same time, this incorrect setting is signaled by the LED Gl 1308 on the front panel of the unit. Rectifier Gl 1305 is preceeded by an inverting amplifier which cancels the inversion provided by IC 1302/4.2. This means that the rectifiers receive the sinusoidal voltage with the same phase.

If operation without the explored range function is desired, the voltage across R 1312 is simply shortcircuited with switch [7] (S 1301).

10.2.11 MEASURING FREQUENCY GENERATION (14)

10.2.11.1 Measuring frequency oscillator 1

The oscillator operates at 10 MHz. Crystal, Q 1406, determines the oscillating frequency; C 1421 is a capacitor for pulling the frequency and is in parallel with trimmer C 1422. The gain of transistor T 1404 is highest at the resonant frequency because there the emitter resistor is short circuited for a.c. At the collector of T 1404 the oscillator signal is shifted in phase by 180° compared to the emitter. Therefore, the oscillating conditions are fulfilled for the oscillator. Choke coil L 1401 lowers the gain at low frequencies and thereby suppresses spurious resonances below the fundamental resonance.

Transistor T 1406 decouples the oscillator voltage and converts it to a TTL singl.

10.2.11.2 Measuring frequency oscillator 2

This oscillator is a Meissner oscillator. The quartz crystals, which provide frequency-dependent feedback in the emitter path, determine the frequency. The resonant frequencies of the quartz crystals lie around 20 MHz and the output signal is subsequently divided in a frequency divider to the required measuring frequency. The various quartz crystals are selected via resistors R 1428...R 1432.

Trimmer capacitors with which various measuring frequencies can be precisely adjusted are connected in series with the quartz crystals. For reasons of phase stability, harmonic quartz crystals are fitted. For this reason, the tuned circuits are fitted in the collector path of the oscillator. The tuned circuit consists of the primary winding of transformer Ü 1401, with capacitors being connected via the control lines R 1407...R 1411, according to the measuring frequency. Each circuit is tuned for maximum amplitude. The corresponding trimmers are C 1408, C 1410, C 1414, and C 1416.

If the RMS-4 is not equipped with the color subcarrier measuring frequency, trimmer C 1414 is set to maximum capacitance. This means that the electrical conditions are changed only slightly if the color subcarrier is installed subsequently.

Diode G1 1402 limits the oscillation amplitude of the oscillator to approx. 7 V_{pp}.

Transistor T 1401, with its associated circuitry, acts as a supply voltage filter - particularly at low frequencies. The corner frequency is approx. 0.3 Hz, resulting in an attenuation of approx. 44 dB at 50 Hz.

The oscillator voltage is extracted from the collector of T 1402 and passed on via transistor stage 1405 to test point TP 1402, where it is available as a TTL signal.

10.2.11.3 Frequency dividers

The frequency divider IC 1401 is supplied with the oscillator frequency of 10 MHz. The divider ratio can be 10:1 or 9:1, resulting in the difference between the measuring frequency series I and II.

This divider is followed by a 2:1 divider and a 3:1 divider and this chain provides the three low measuring frequencies with twice the required value.

The flip-flop IC 1404/2.2 which divides the frequency by a further factor of two is at the output of the circuit. This flip-flop always provides a duty cycle of 1:1, as this is prerequisite for the following circuit in assembly (15).

If the three low measuring frequencies are not selected by the measuring frequency switch, then IC 1401 sets its output "High" via a logic circuit.

The 500 kHz frequency for assemblies (17) and (8) and 50 kHz for assembly (12) are also obtained from the measuring frequency oscillator 1 via IC 1405, IC 1406, and IC 1408.

The high measuring frequencies are generated from the measuring oscillator 2. In the normal version of the unit, these are the four measuring frequencies 12.39 MHz (from 24.78 MHz), 8.2 MHz (from 16.4 MHz), 5.6 MHz (from 22.4 MHz), and 2.4 MHz (from 19.2 MHz).

The color subcarrier frequencies 3.579545 MHz, 3.580 MHz, 4.430 MHz, or 4.433618 MHz (all extracted from 4 times the required frequency) can be fitted as an optional feature.

It is also possible to install other frequencies in the range 2.0 MHz ... 12.39 MHz to special order. Unused diode positions are provided for the logic circuit.

As the measuring frequencies in some cases are derived from a multiple of their nominal frequency, they must be divided. The flip-flop IC 1404/2.2 at the output of the circuit already divides by a factor of 2. This means that the frequencies 23.78 MHz and 16.4 MHz can be connected directly to IC 1403/4.4.

22.4 MHz and 4-times the color subcarrier frequency are divided by a factor of 2 by IC 1402/2.1.
19.2 MHz is divided by a factor of 4 by IC 1402/2.1-2.2.

The output of IC 1402/2.2 is "Low" due to the logic circuit. Only when the 2.4 MHz measuring frequency is selected with switch [19] (S 1501) is the flip-flop activated.

The output of IC 1402/2.1 is switched to "Low" if the 12.39 MHz or 8.2 MHz measuring frequency is selected.

This switching of the flip-flops means that the measuring frequencies are in some cases no longer present on some lines, thus avoiding cross talk between the frequencies.

Only one measuring frequency is active at any time. This is achieved by means of logic circuits which open only one gate of IC 1403 or IC 1407 at one time.

At the output of IC 1402/2.2, the voltage sweep is reduced by a factor of 5 by the divider R 1447/R 1452 before the measuring signal is connected to pin (14) 71 or to assembly (15).

This avoids cross talk in assembly (15), which could result in a linearity error of the measuring voltage.

10.2.12. U_M AMPLIFIER, U_M CONTROL ELEMENT (15)

10.2.12.1 U_M control element

The U_M control element has the task of converting the TTL signal coming from the measuring frequency generation (14) into a signal with a variable amplitude. The measuring voltage sweep at the output of the unit can be adjusted between 0 and 500 mV_{rms} with potentiometer [14] (P 1501).

The incoming square-wave signal is processed by the limiter T 1501 and T 1502. The current through the limiter or through T 1502 results in a defined AC voltage drop across R 1508. This current is set up by the input voltage G1 1501-tap of P 1501, and is also present across the series circuit R 1506, P 1502.

Potentiometer P 1502 is adjusted during calibration of potentiometer [16] (P 1501).

If the "gap" is used, the square-wave signal from assembly (13) is differentiated by C 1555/R 1506 and connected to transistor T 1527. This transistor conducts momentarily via R 1507 and reduces the voltage across potentiometer [16] (P 1501), which means that the measuring voltage U_M is also reduced momentarily. The use of the "gap" was described in the description of assembly (13).

10.2.12.2 U_M amplifier

This module consists basically of 8 separate common collector stages which couple the measuring signal to transistor T 1522 via a tuned series resonant circuit.

Transistor T 1522 operates in a common base circuit; the resistive component of the series circuit acts as an input impedance. The gain of the common base circuit is maximum in the case of resonance.

Due to the deviations in the components which participate in generating the input impedance of the common base stage, the input impedance must be adjusted to a specific value (40 Ω) with potentiometers P 1503...P 1509. The preceding common collector stages T 1505, T 1507, T 1509, T 1512, T 1514, T 1516, T 1518, T 1520 are activated separately - according to the measuring frequency - via the measuring frequency switch [19] (S 1501) and the transistor stages T 1506, T 1508, T 1510, T 1513, T 1515, T 1517, T 1519, and T 1521 in the base and collector circuits.

As functions in assemblies (13) and (14) are simultaneously initiated by the measuring frequency switch [19] (S 1501) a simplified circuit diagram (Figure 10-7) is used to explain the basic principle of operation of the measuring frequency switch.

Principle of operation of the measuring frequency switch [19] (S 1501)

All measuring frequencies of the unit can be selected "internally" or "externally".

The decision as to whether internal or external measuring frequency selection is to be carried out is provided by activation of transistor stage T 1511. Internal selection of the various measuring frequencies is carried out via the leads from switch [19] (S 1501) to the U_M amplifier.

The external selection is carried out via the parallel leads from socket [30] (Bu 1501) to the U_M amplifier.

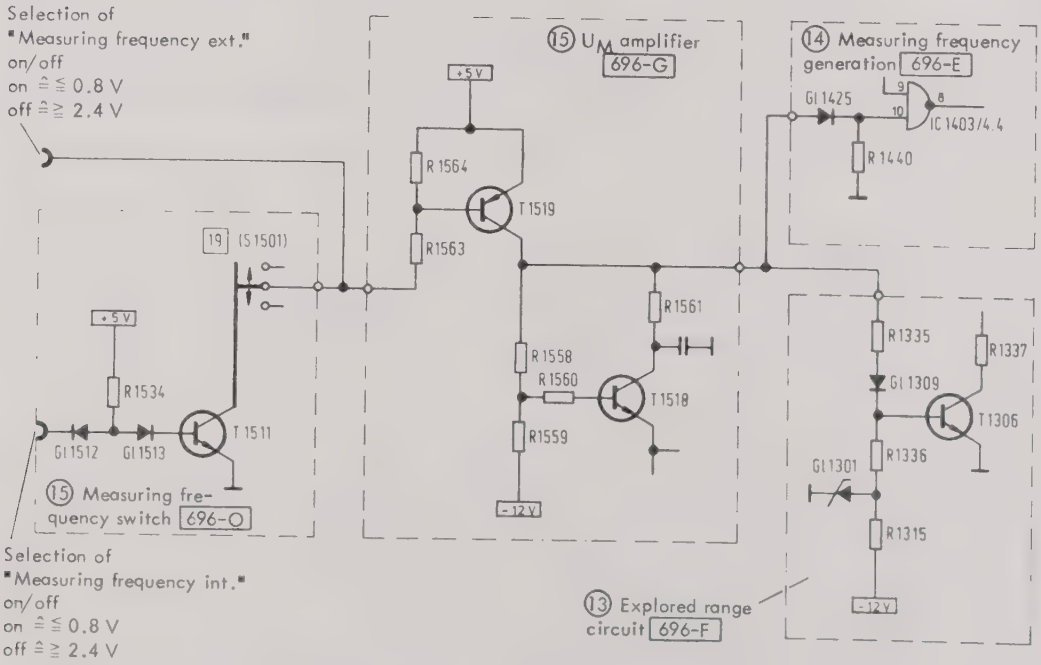

Figure 10-7 Principle of operation of the measuring frequency switch S 1501, shown for the measuring frequency 8.2 MHz

If the 8.2 MHz measuring frequency is selected, transistor T 1519 conducts. The positive DC potential (+4.5 V) at the collector switches on transistors T 1518 and T 1306, and the gate IC 1403/4.4 is also activated. The measuring frequency passes through this gate and through the following circuit to transistor T 1518.

At the same time, the deflection signal U_A in assembly (13) is divided according to the selected measuring frequency.

Amplifier stage

The output from the amplifier stage with an output impedance of $R_i \approx 0$ and a full level is 1 V. The level across R_A = 75 Ω is 500 mV, a result of the output impedance in assembly (16).

The measuring voltage arriving at test point TP 1502 is connected to a low-pass filter with a limit frequency of 15 MHz. Resistors R 1581 and R 1587 provide termination for the low-pass filter. The value of R 1587 is higher because the input resistance of transistor T 1523 is connected parallel to this resistor.

T 1523 and T 1524 form a differential amplifier. T 1524 drives the complementary output stage T 1525, T 1526. The output is fed back through R 15108 to the base of T 1524. The overall stage gain is slightly less than 1 owing to the loop gain being finite.

The total gain of the circuit from input to output is shwon in a simplified form in Figure 10-8.

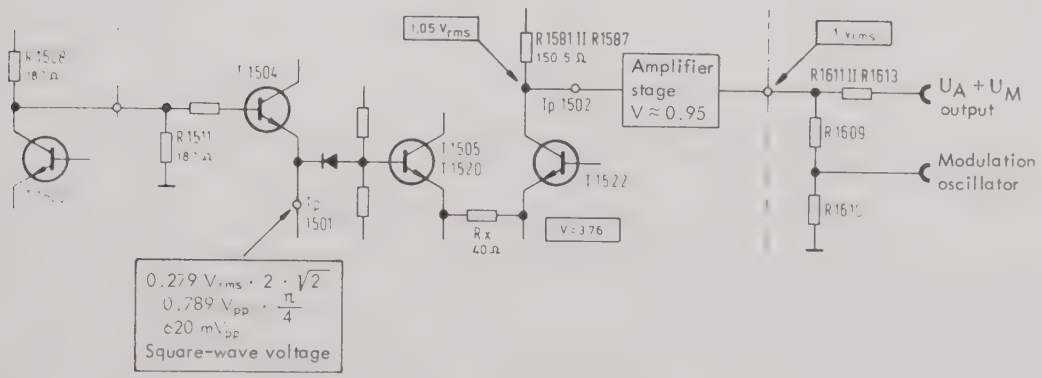

Figure 10-8 Level diagram of the complete U_M amplifier

10.2.13 OUTPUT SWITCH, 2 x 20 dB ATTENUATOR, U_M changeover switch (16)

From the slider potentiometer [17] P 1305 is fed the deflection voltage to amplifier IC 1601, which drives the output stage transistors T 1608 and T 1609. This is a complementary pair, class B mode output stage. Inverse feedback through R 1601 and R 1602 establishes the gain and the d.c. output voltage 0 V.

In order to handle the large voltage swing of 10 V at the output, the supply voltage must be $\pm$ 16 V. The stabilization circuit for this voltage is located on the printed circuit board of assembly (9).

Through relay contact rel 1601, which switches off the deflection voltage in specific operating situations, the deflection voltage is fed to a voltage node. From this point the voltage is routed to both the assembly (9) (frequency stabilization) and the parallel circuit R 1616, R 1617 that forms the output resistance. Behind the succeeding low-pass filter with the cut-off frequency of $\approx$ 6 kHz the measuring voltage is added, and the summation signal $\hat{U}_A + U_M$ is connected to the output [14] (Bu 1605) via the attenuator switch S 1601/2.2 that attenuates the summation signal by 0 dB or by 20 dB, as selected.

The measuring voltage from point (16) 33 is applied to the addition point where the deflection voltage is also applied. But the measuring voltage can be switch selected for 0 dB or 20 dB attenuation by S 1601/2.1, the attenuation switch, located before the high-pass filter of $\approx$ 5 kHz cut-off.

Rel 1602 has the task of switching off the internal measuring signal when the unit is operated in wideband mode. However, due to the high requirements for disconnection of this signal, further measures are necessary. The measuring signal is simultaneously short-circuited at R 1611 with rel 1602 and in the U_M changeover switch with T 1605.

10.2.13.1 Control of the deflection voltage U_A

The term "control" refers to switching on and off of the deflection voltage U_A with relay Rel 1601. Various functions cause the deflection voltage to be switched off:

- If the measuring frequency f_M is greater than the selected explored range $\hat{\Delta F}_A$, then the deflection voltage must be switched off. LED G1 1308 signals this optically ($f_M \geqq \Delta F$). The voltage at amplifier IC 1302/4.4 drops to approx. 9 V and causes a current to flow through the

relay coil Rel 1601, Gl 1602, and Gl 1601. The Zener diode Gl 1602 prevents a) excessive voltage drop across the relay coil, b) the relay from opening before the indicator Gl 1308 ($f_M \cong \Delta F$) lights.

- If the center frequency is calibrated in the IF section with the switch [4] (S 803), then the deflection voltage must be switched off for calibration reasons. In this case, Gl 1603 is connected to ground via switch [4] (S 803/D) in the position "CAL". The relay coil Rel 1601 is energized.
- The transistor stage T 1603 is switched on for speech traffic via the headset socket [33] (Bu 1604). This causes Rel 1604 in the U_M changeover switch to switch to the headset input. At the same time, assembly (9) is switched via a logic circuit to wideband mode. Similarly, the deflection voltage U_A is switched off through Gl 1606 by Rel. 1601.

10.2.13.2 Control of the measuring voltage U_M

Control of the measuring voltage consists of switching off the measuring voltage in certain operating cases.

- The RMS-4 can be set to wideband mode with switch [8] (S 902/II). The measuring voltage is then connected externally. This is done by activating relay Rel 1603. In order to prove the necessary isolation, the internal measuring voltage is also short-circuited by transistor Rel 1602. In U_M changeover switch, the line is additionally short-circuited by transistor T 1605. These switching functions are initiated only by the switch [8] (S 902/II).
- The same switching functions can be initiated if switch [34] (S 901/II) is set to "U_A, U_M ext." or if switch [4] (S 803/D) is set to "CAL".

10.2.14 IF CALIBRATION GENERATOR 70 AND 140 MHz (18)

The IF calibration generator consists of the printed circuit boards 70/140 MHz oscillator and phase measuring circuit, the two being connected together by a phase control circuit. The oscillator is formed by the transistor stages T 1814, and T 1818. Their emitters are connected together via the series resonant circuit L 1810, L 1811, and C 1842, GL 1812. The signal is fed back from the collector of T 1818 to the base of T 1814 via R 1847, C 1836.

Frequency switching between 70 MHz and 140 MHz is carried out by switching diode Gl 1808, which short-circuits L 1810, C 1837. The diode is controlled from pin 124 via T 1811, T 1813, T 1817, T 1815, and T 1816. For f = 70 MHz, the current from T 1814 flows via Gl 1807, T 1846, T 1815 to the negative supply voltage. For f = 140 MHz, the current flows through Gl 1808, Gl 1810, R 1848, and T 1816 to $-U_B$.

The oscillator voltage is connected from the collector of T 1814 to the IF_0 output via T 1810 and a low-pass filter. It is also connected via T 1812 and a 50 Ω T element from pin 127 to the phase measuring circuit. From here, the control voltage is connected via IC 1806 with correction circuit and a 220 kHz low-pass filter to the capacitance diode Gl 1812, thus closing the phase control loop.

The low-pass filter is provided to prevent the 1 MHz output voltage of the phase measuring circuit from reaching the capacitance diode.

The current through the oscillator transistors, and thus the output level, can be adjusted with P 1801. The frequency response between 70 MHz and 140 MHz can be adjusted with C 1839. The oscillator voltage from pin 127 is connected via pin 111, the amplifier stages T 1801 and T 1802, a divider chain, and an exclusive OR circuit IC 1805 to the phase measuring circuit. The division ratio can be switched between 280:1 and 140:1 by a signal at pin 116. This means that pin 5 of IC 1805 has a 500 kHz voltage whose phase is compared with the measuring frequency voltage at pin 4 of IC 1805. The deviation at pin 6 is connected via decoupling stages and current sources T 1806, T 1807 and via the integration circuit C 1824, R 1872 to the AGC amplifier IC 1806 (pin 119 in the oscillator section).

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